**FIG. 1**

2807.2.4.10

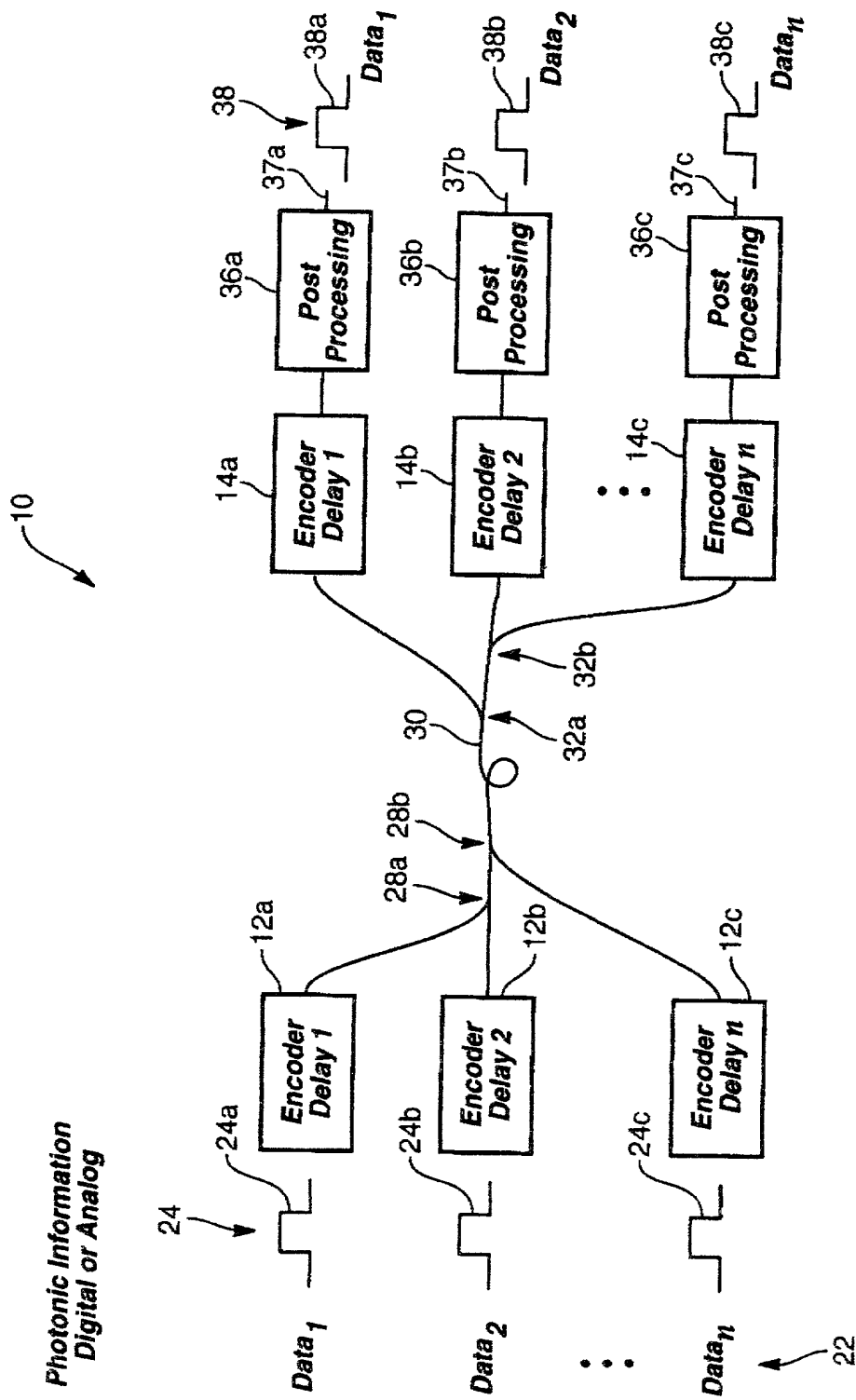
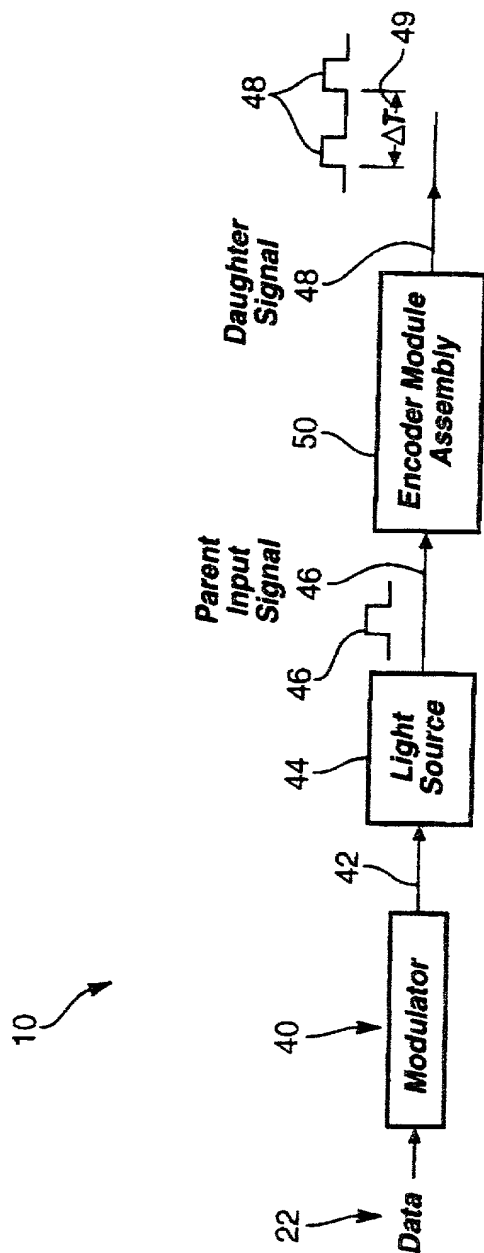


Fig. 2

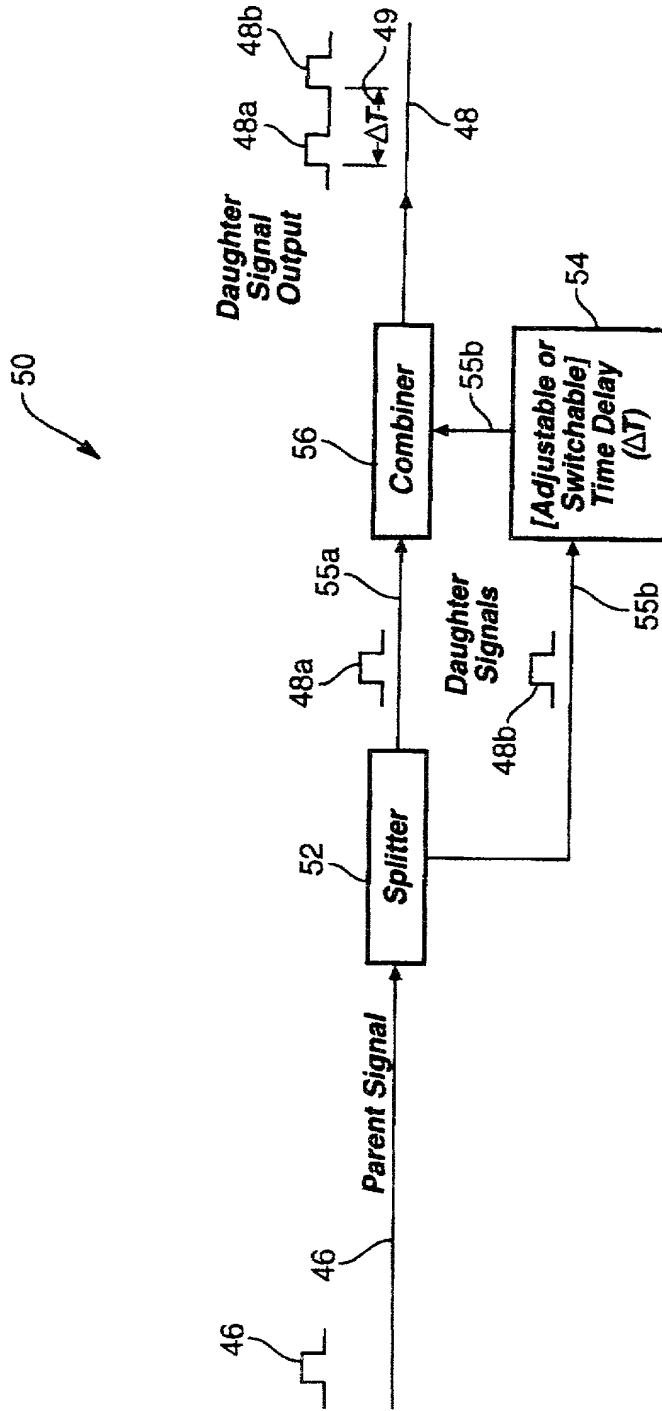
2807.2.4.10



Differential Delay Multiplexer Sender/Encoder

Fig. 3

2807.2.4.10



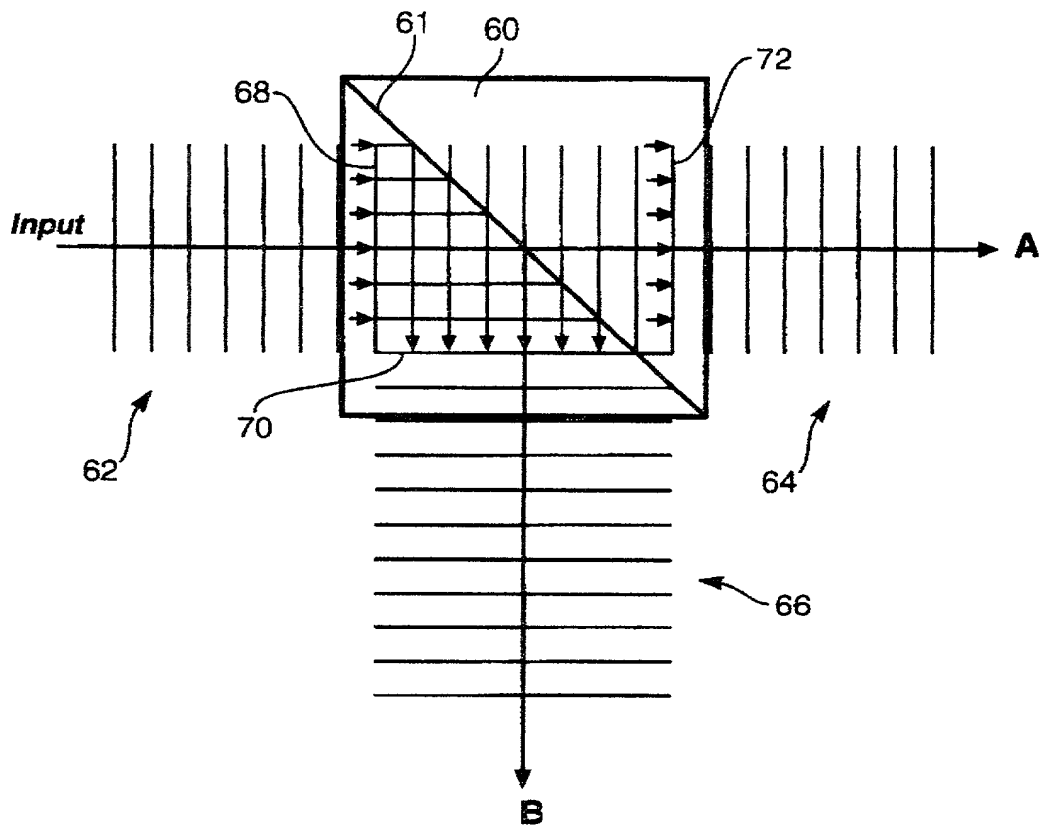
Differential Delay Multiplexer (DDM) Sender/Encoder

Fig. 4

2807.2.4.



2807.2.4.



Amplitude or Polarization Splitter

FIG. 7

2807.2.4.

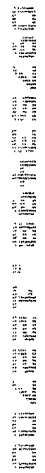
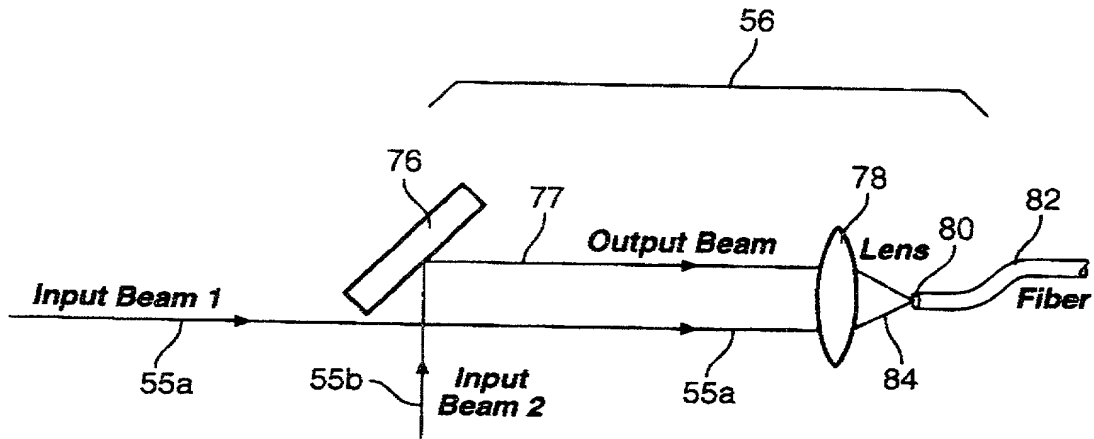
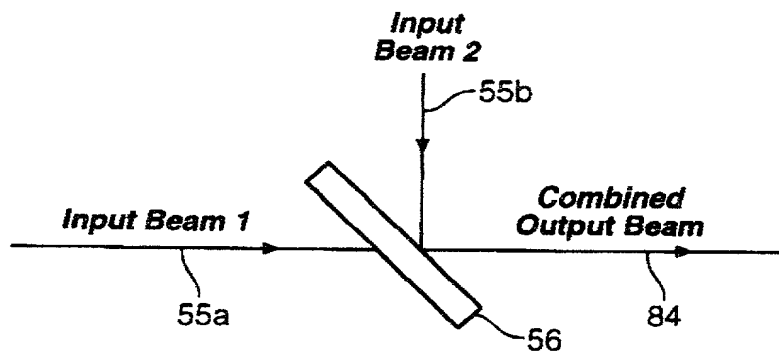


FIG. 7A

2807.2.4.



Beam Combiner
FIG. 8



Amplitude or Polarization Combiner

FIG. 9

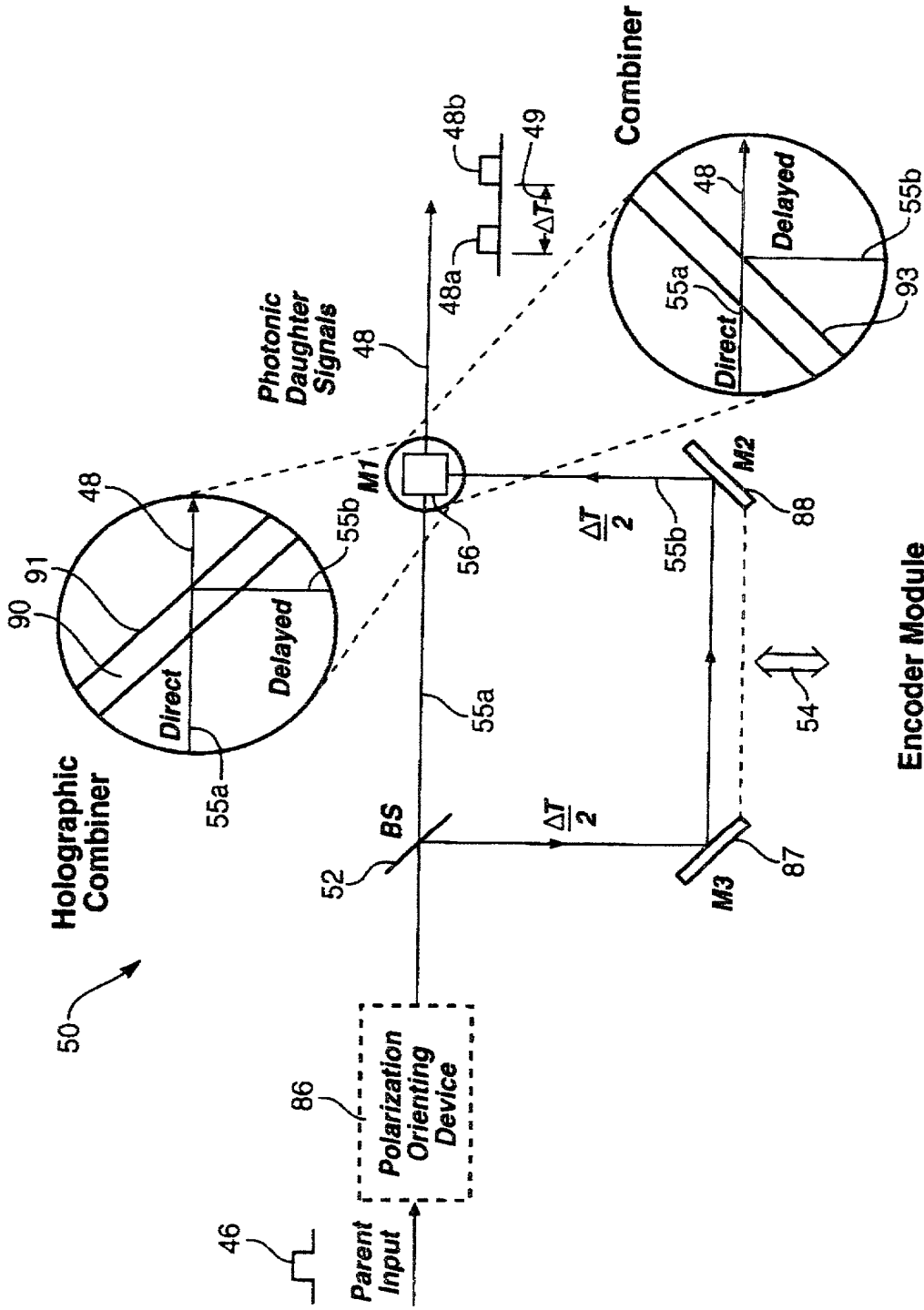
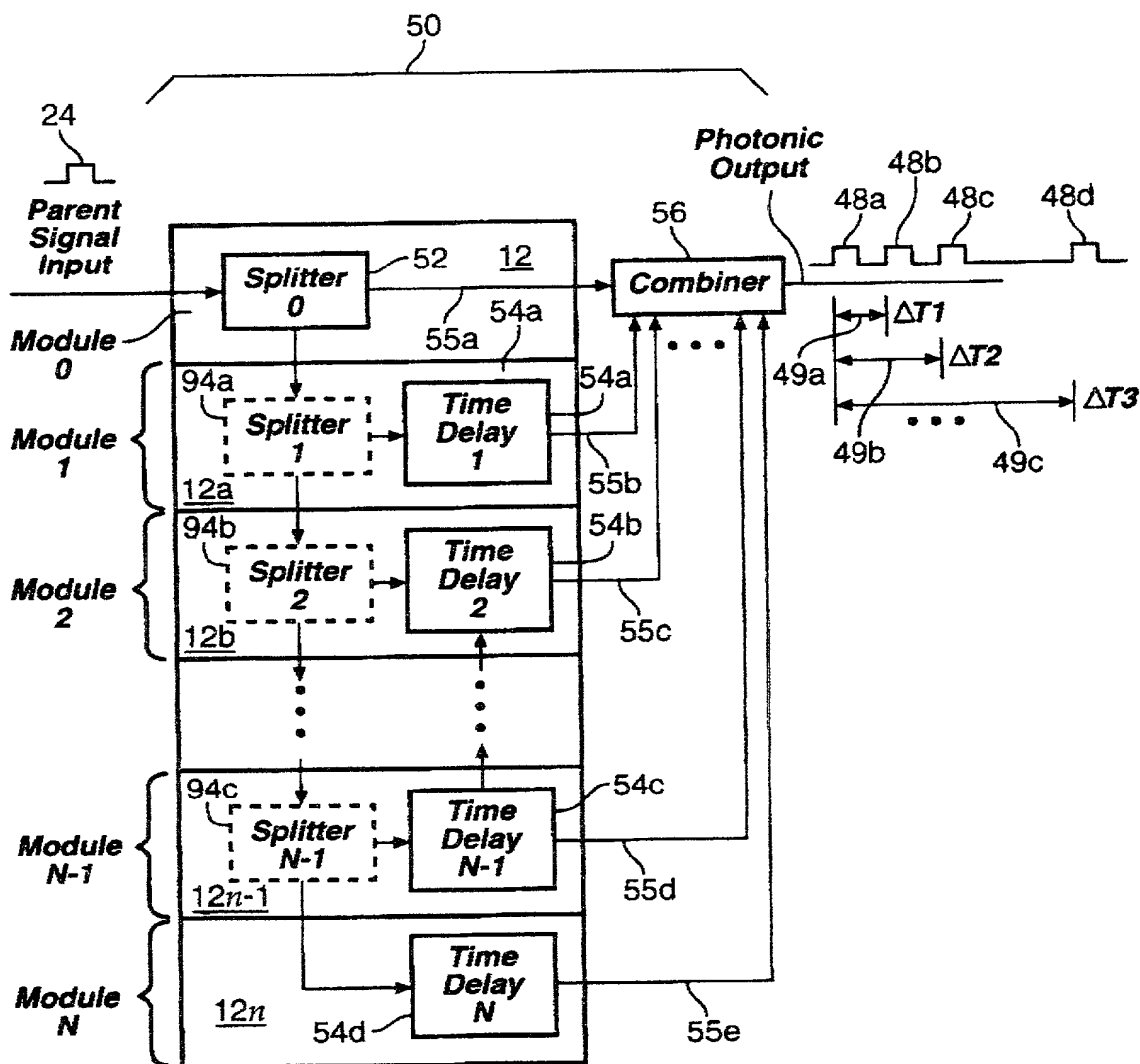


Fig. 10

2807.2.4.



Composite Encoder
Module Assembly

FIG. 11

2807.2.4.

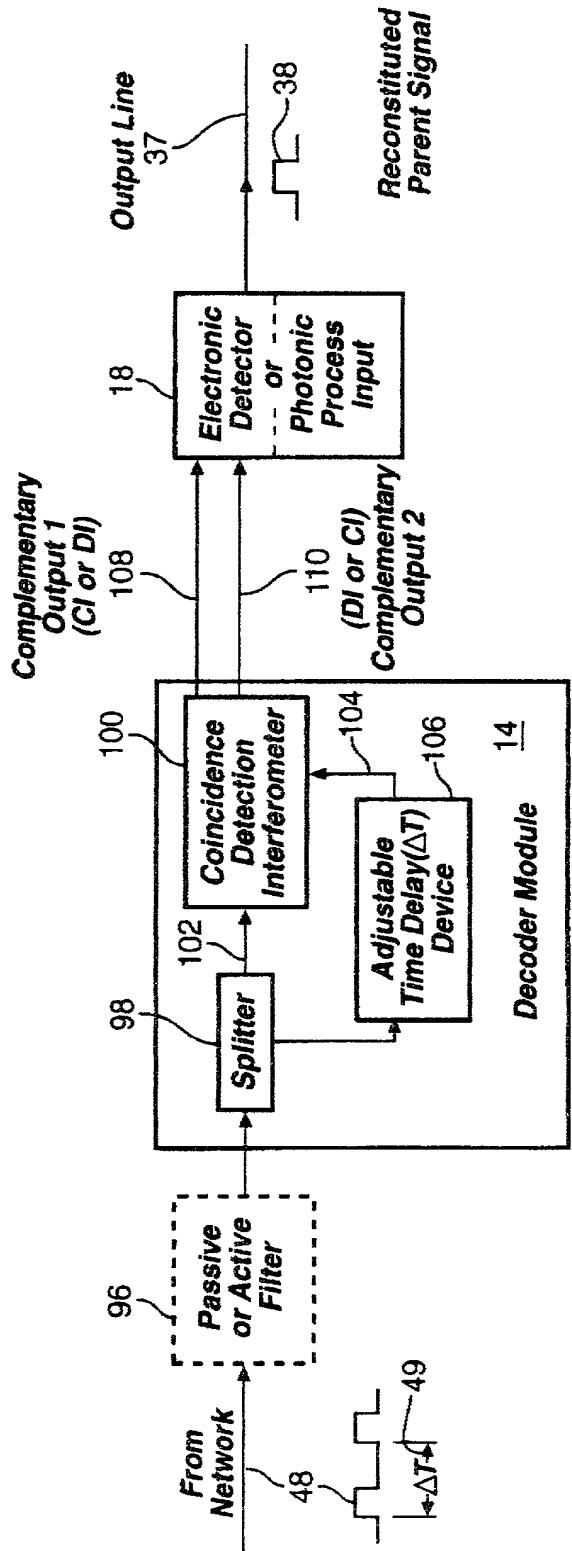


Fig. 12

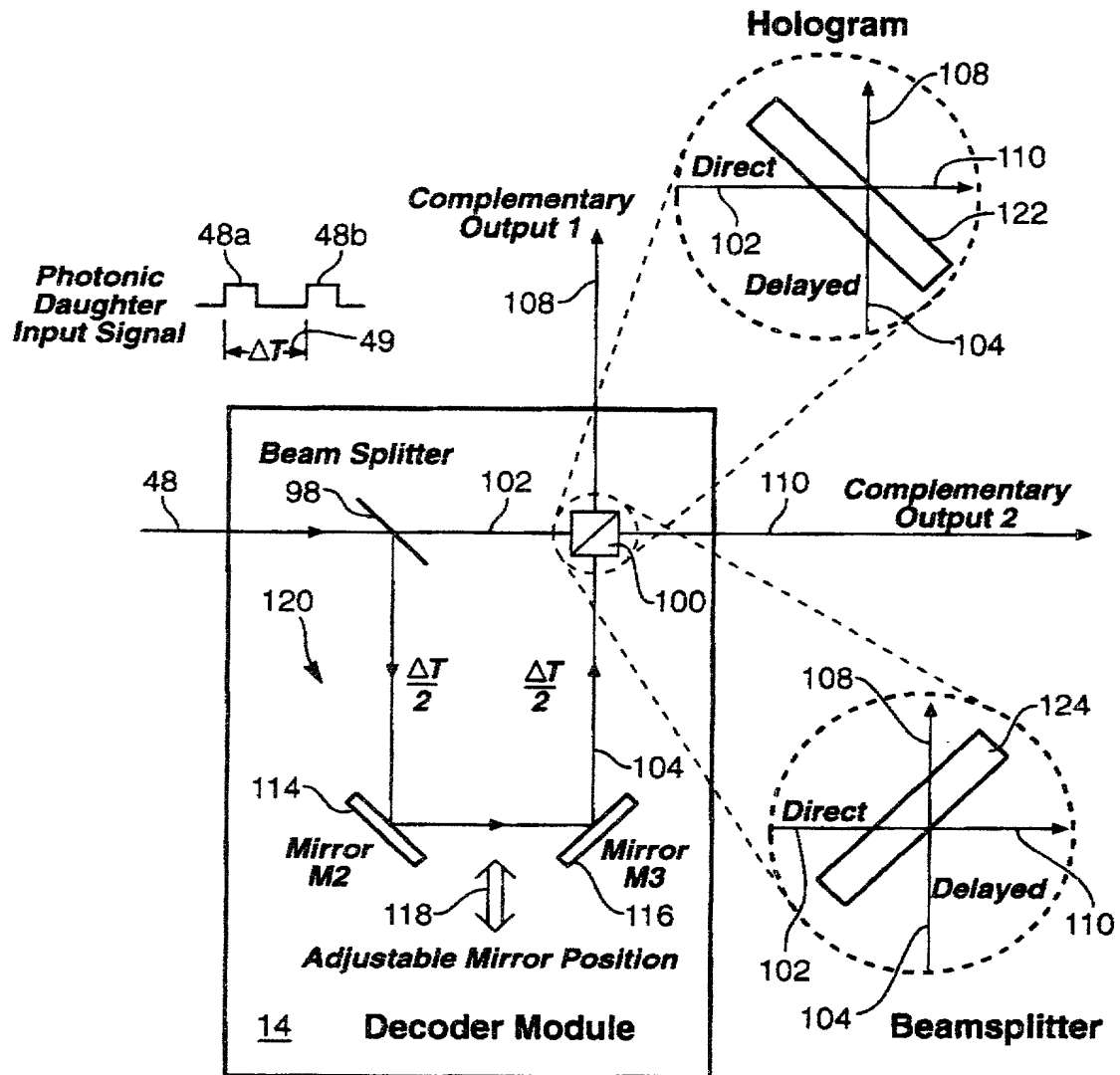


FIG. 13

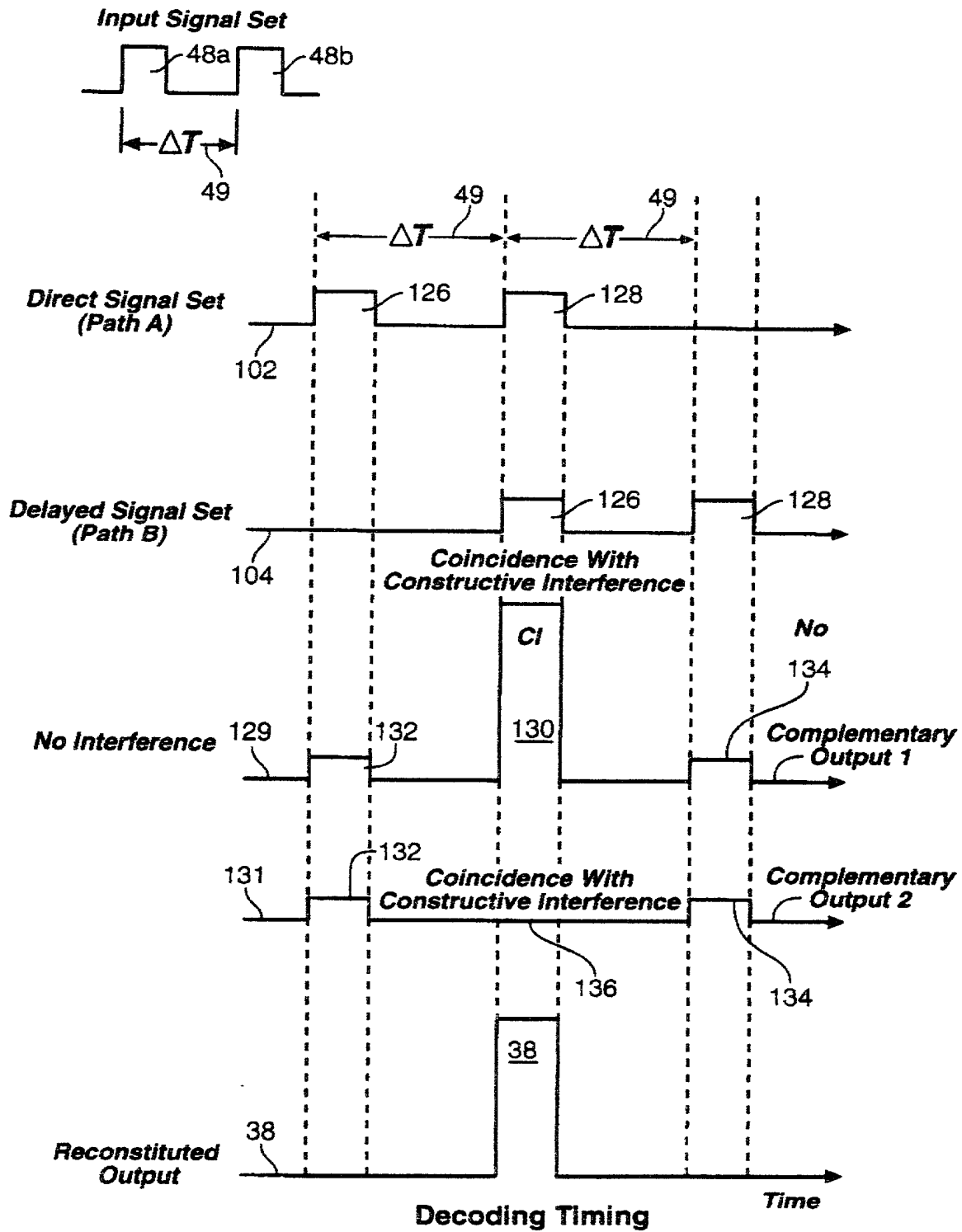


FIG. 14

48

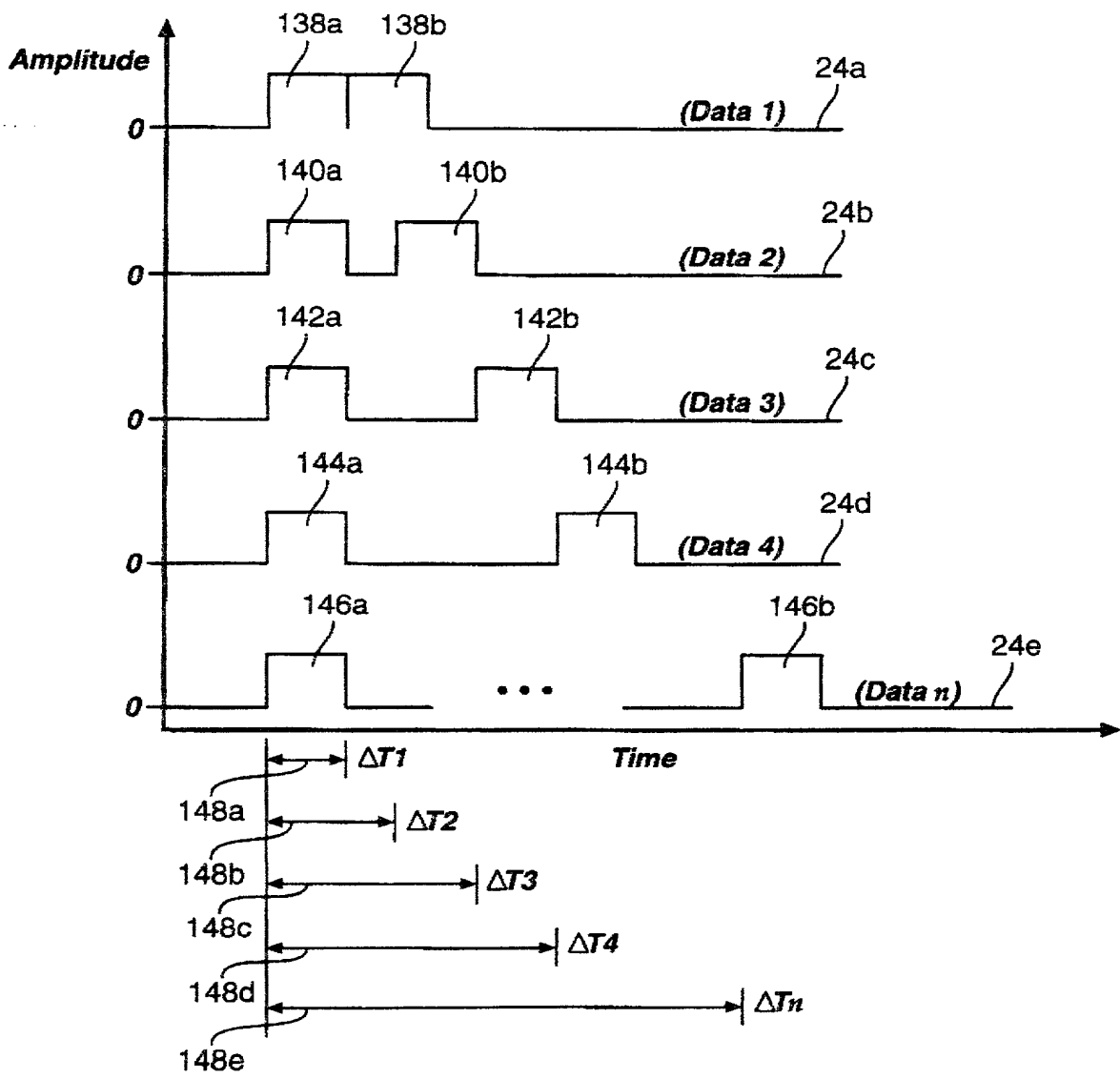


Fig. 15

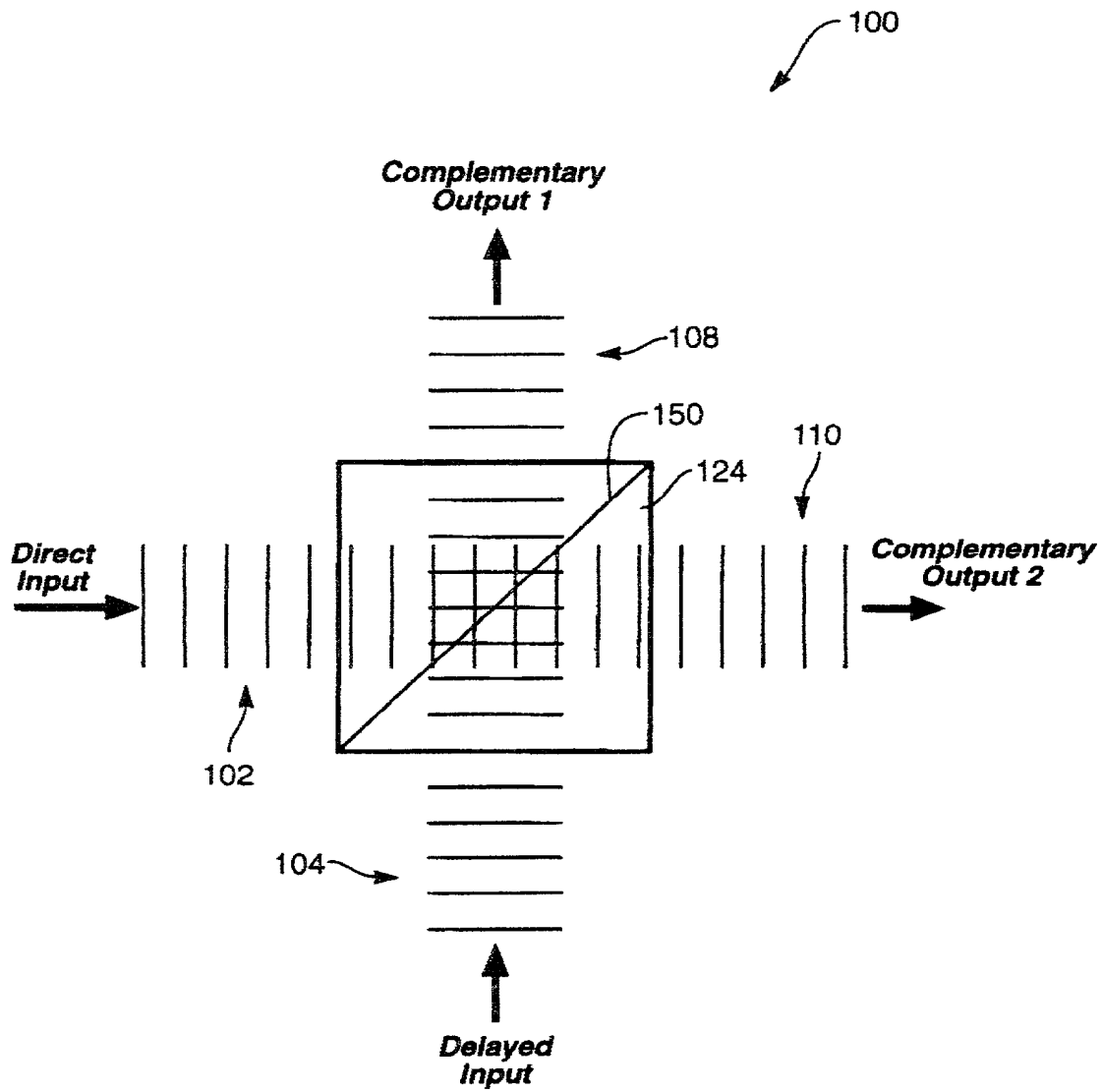


Fig. 16

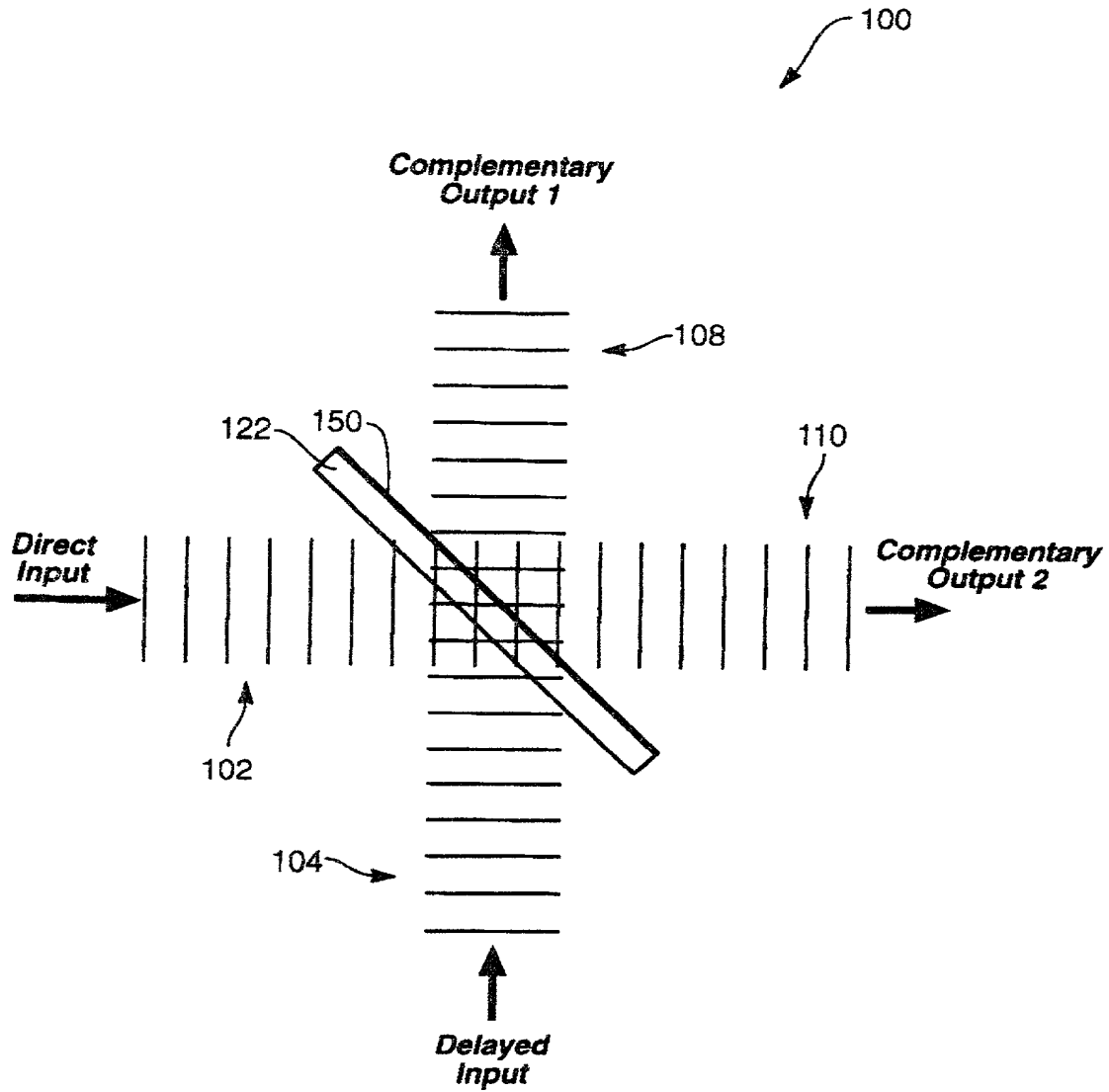


Fig. 17

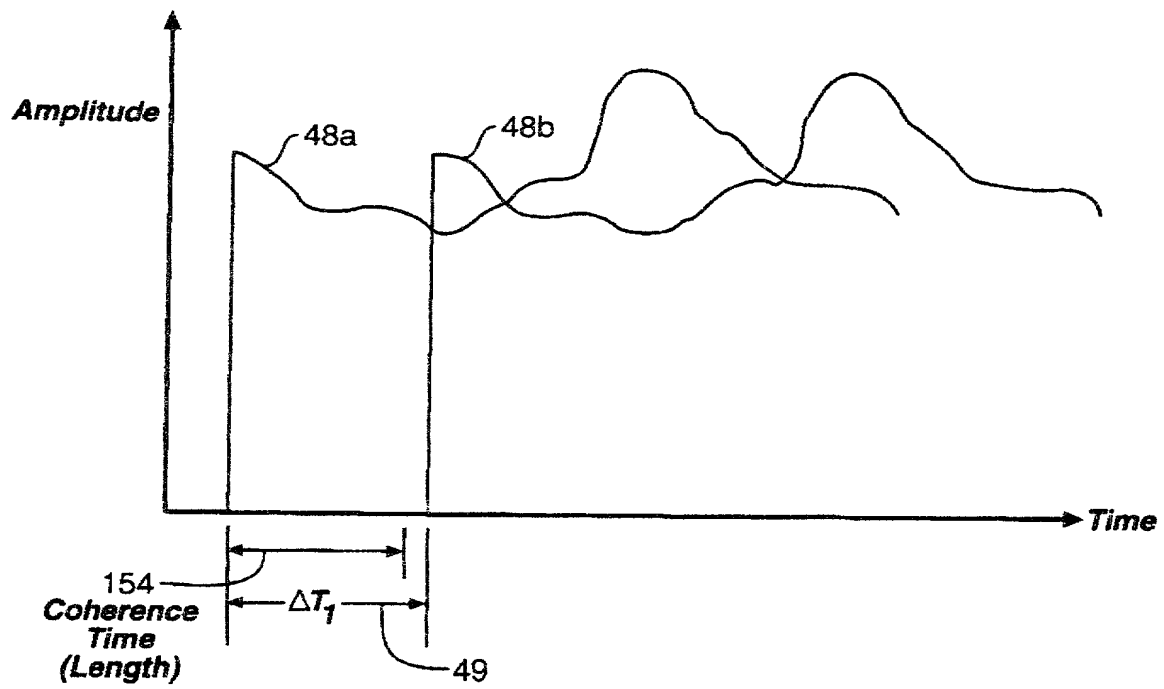


Fig. 18

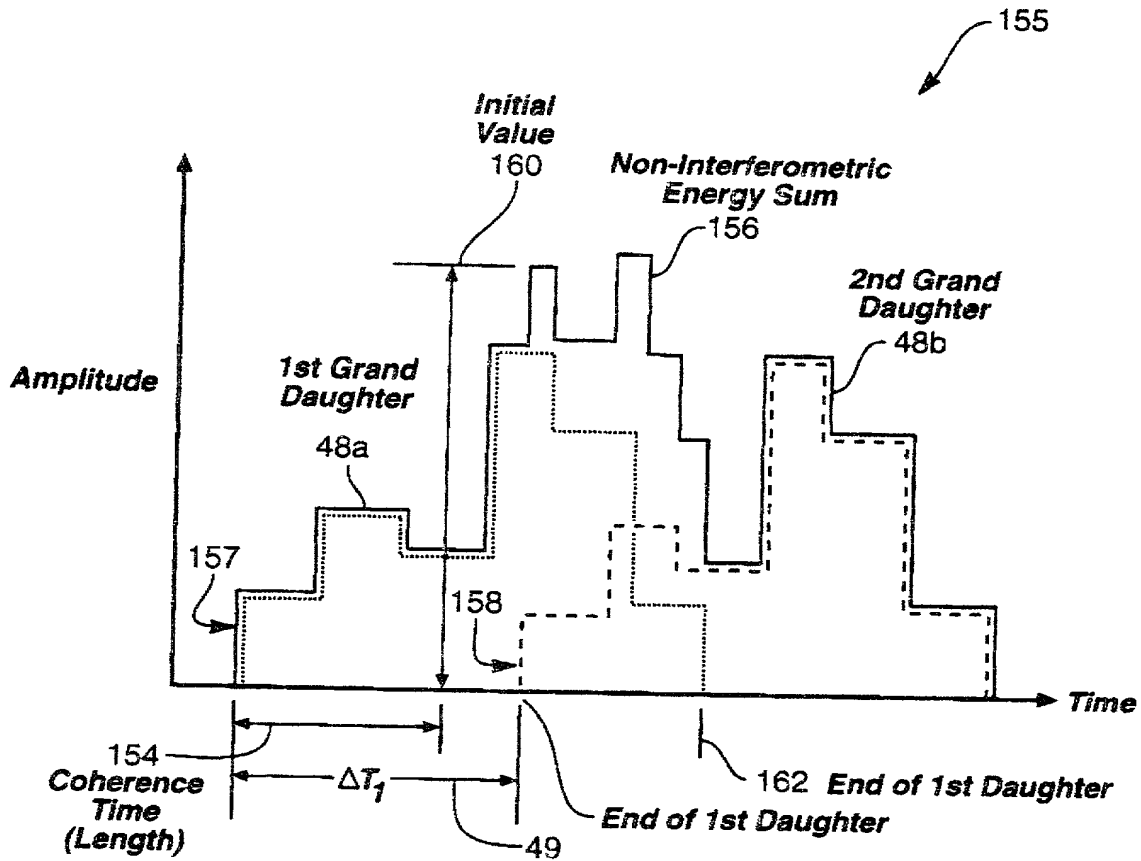


Fig. 19

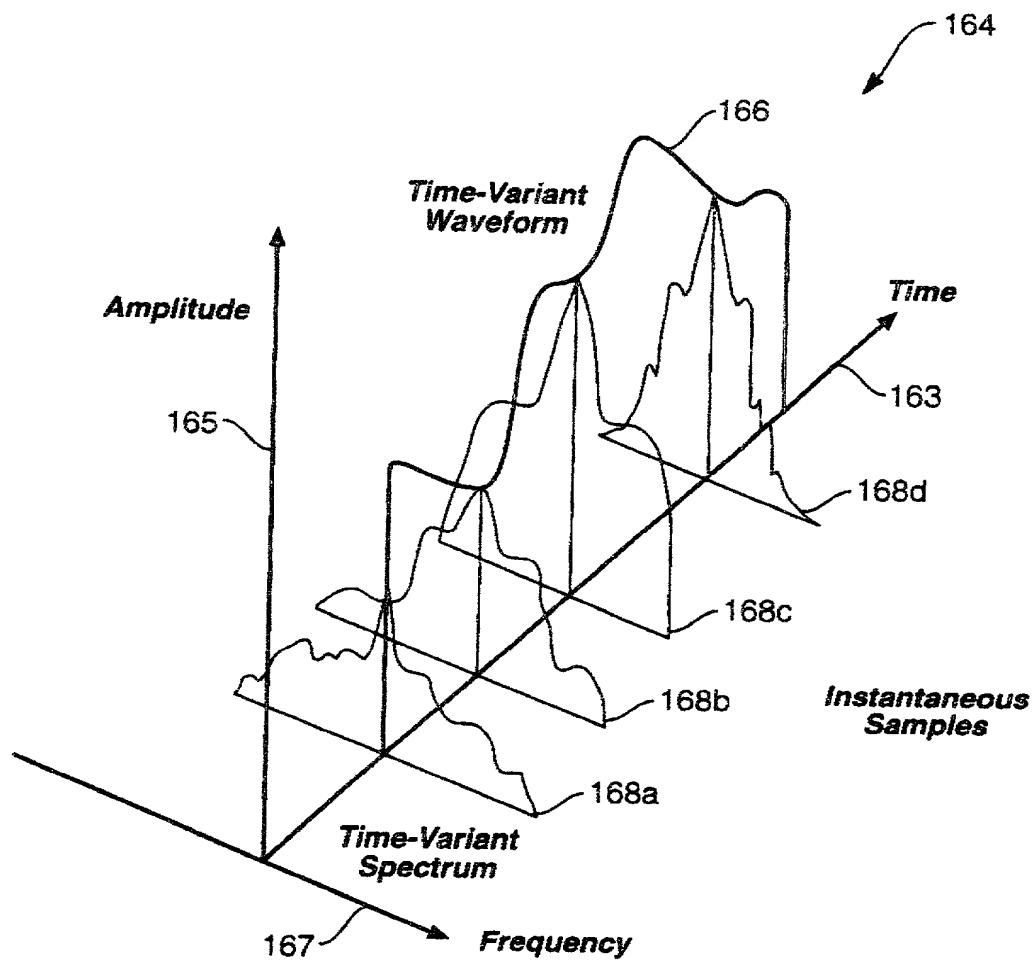
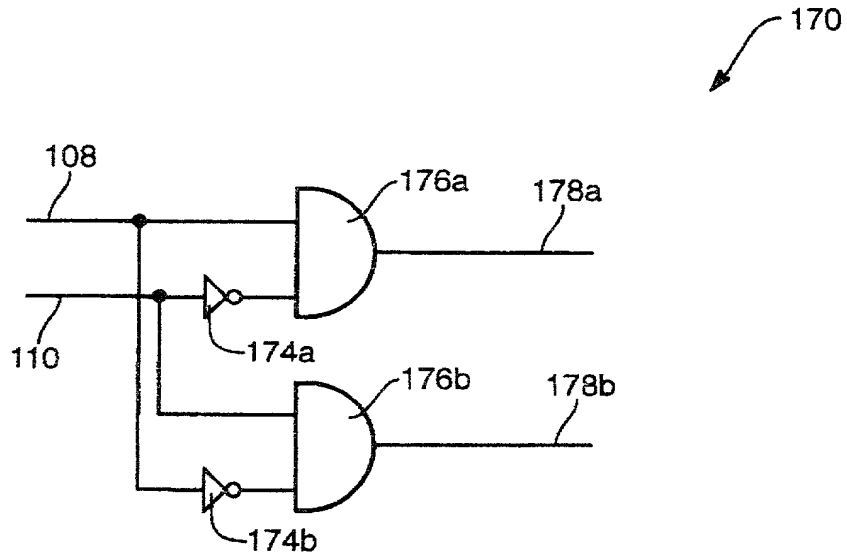
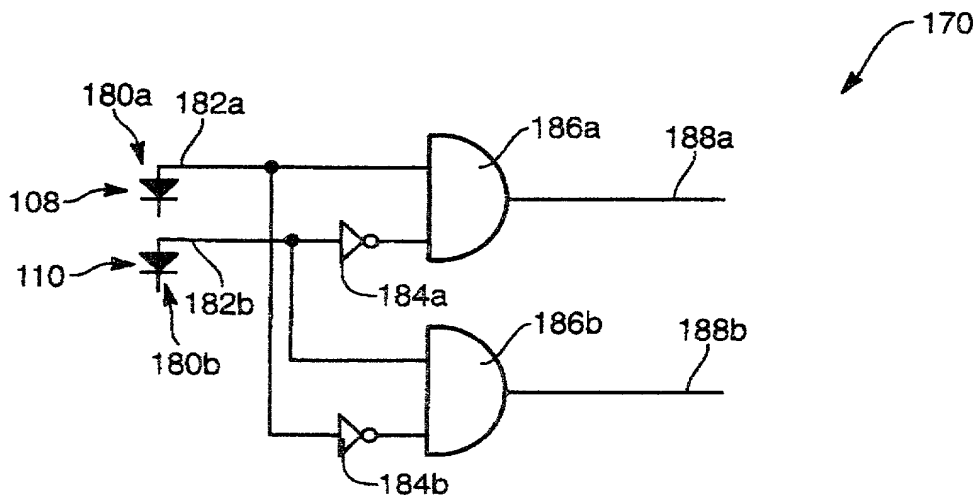


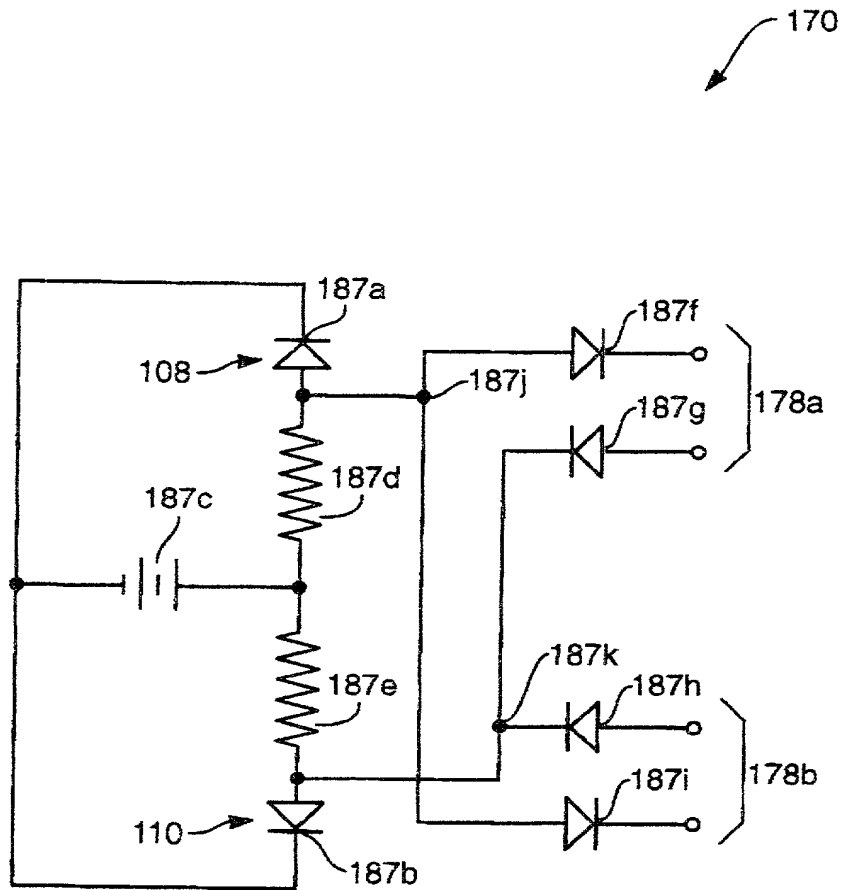
Fig. 20



Photonic Processor
Fig. 22

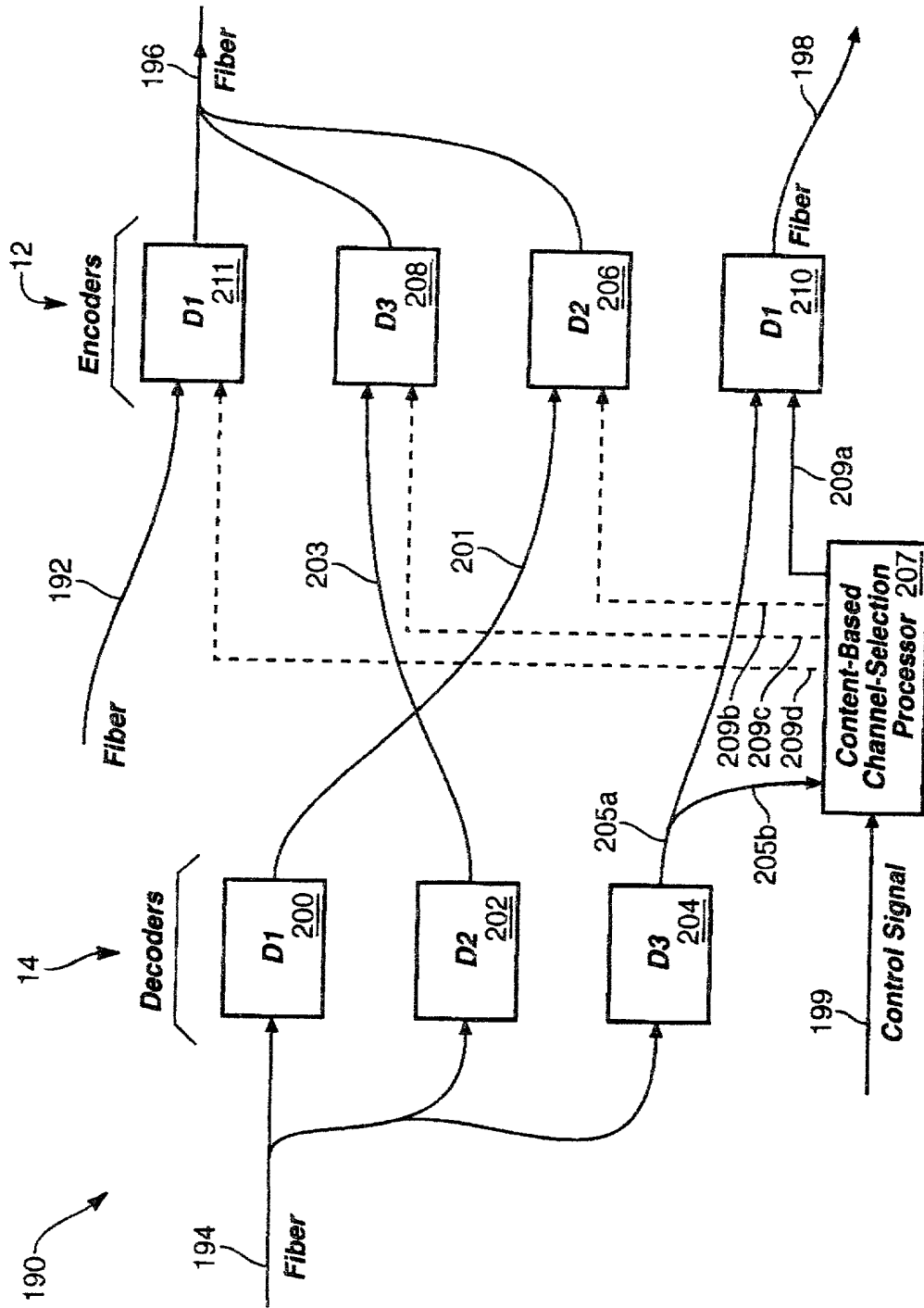


Electronic Processor
Fig. 23A



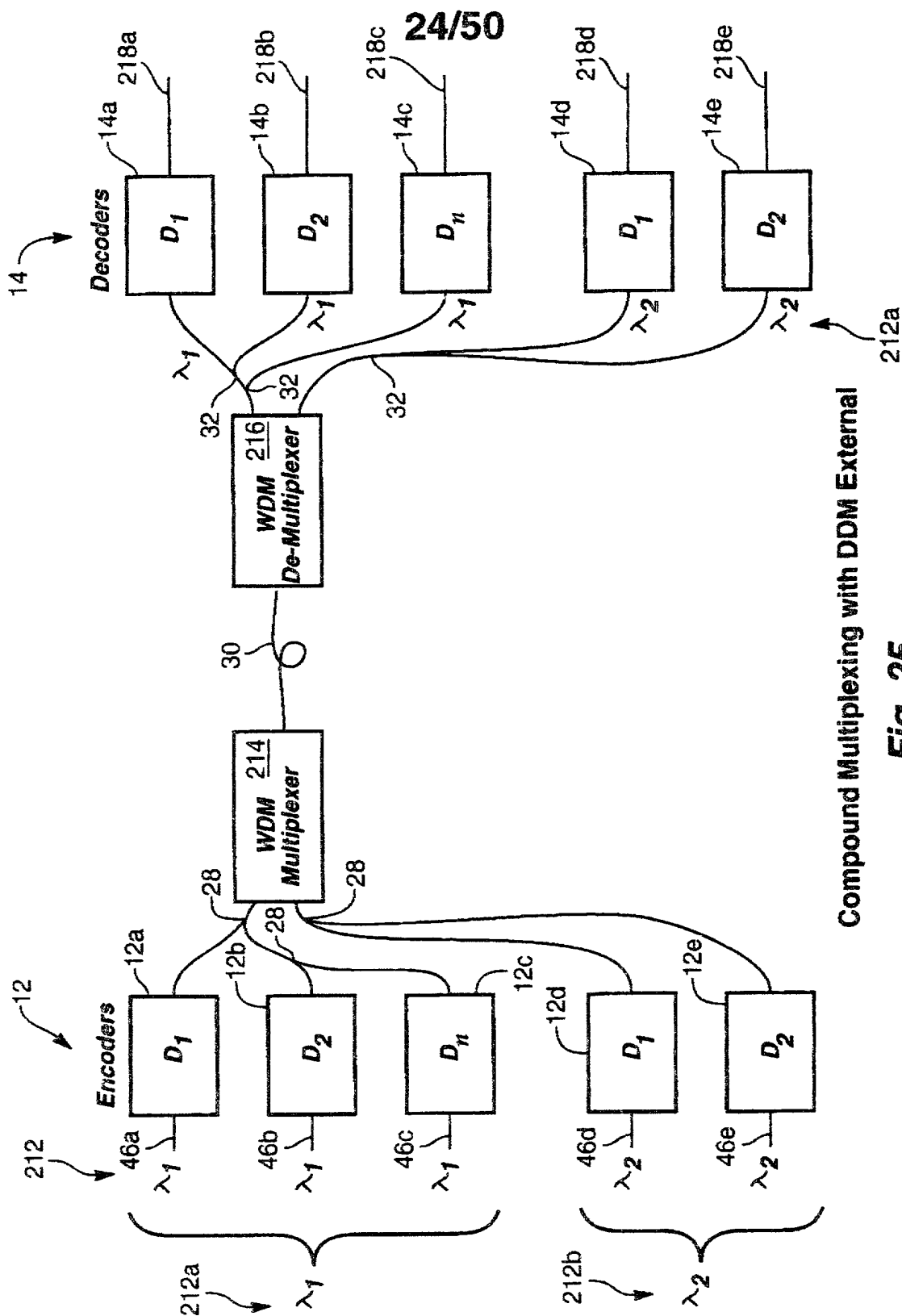
Electronic Processor

Fig. 23B



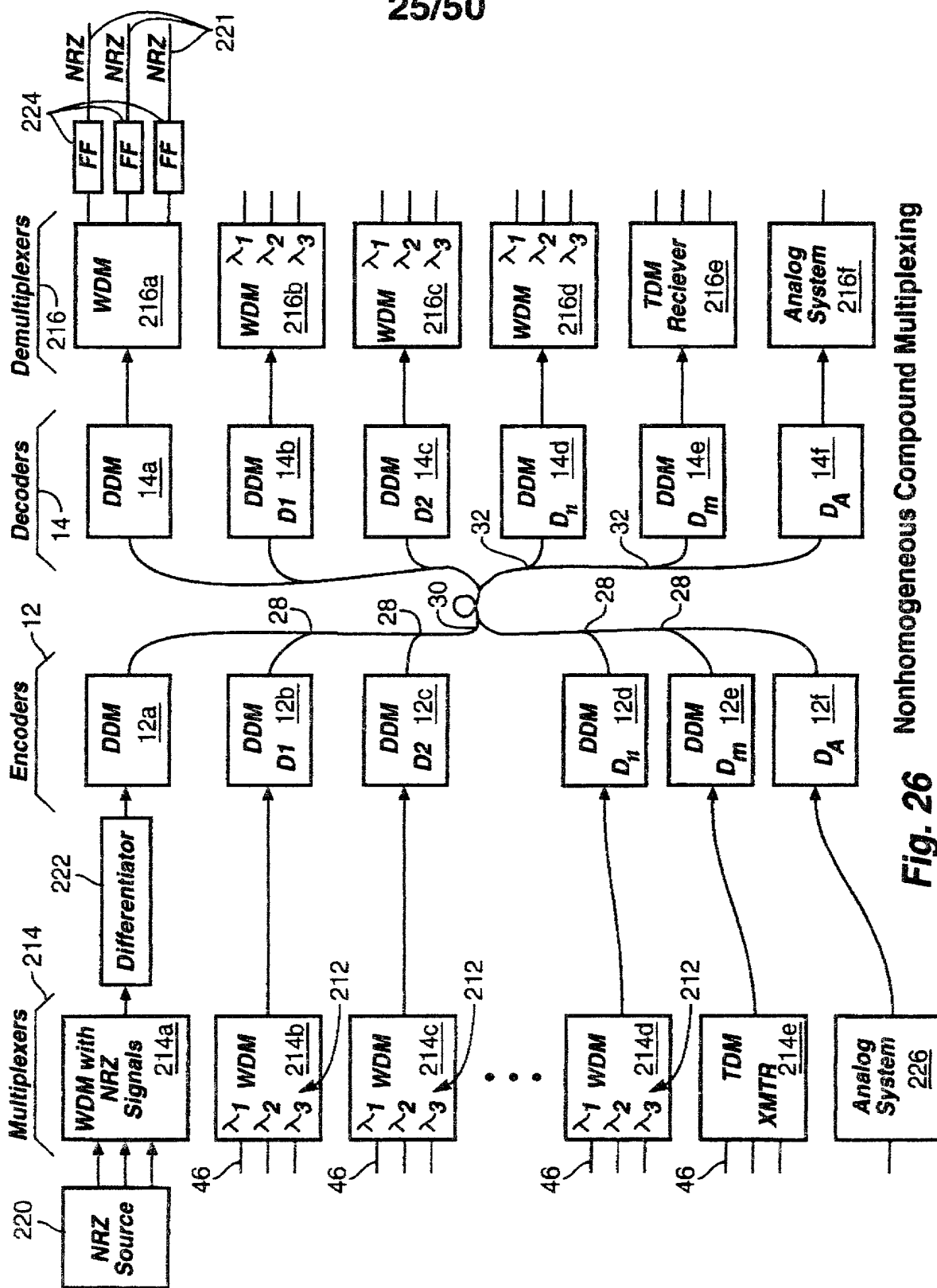
Drop/Rearrange/Add Unbuilding/Rebuilding

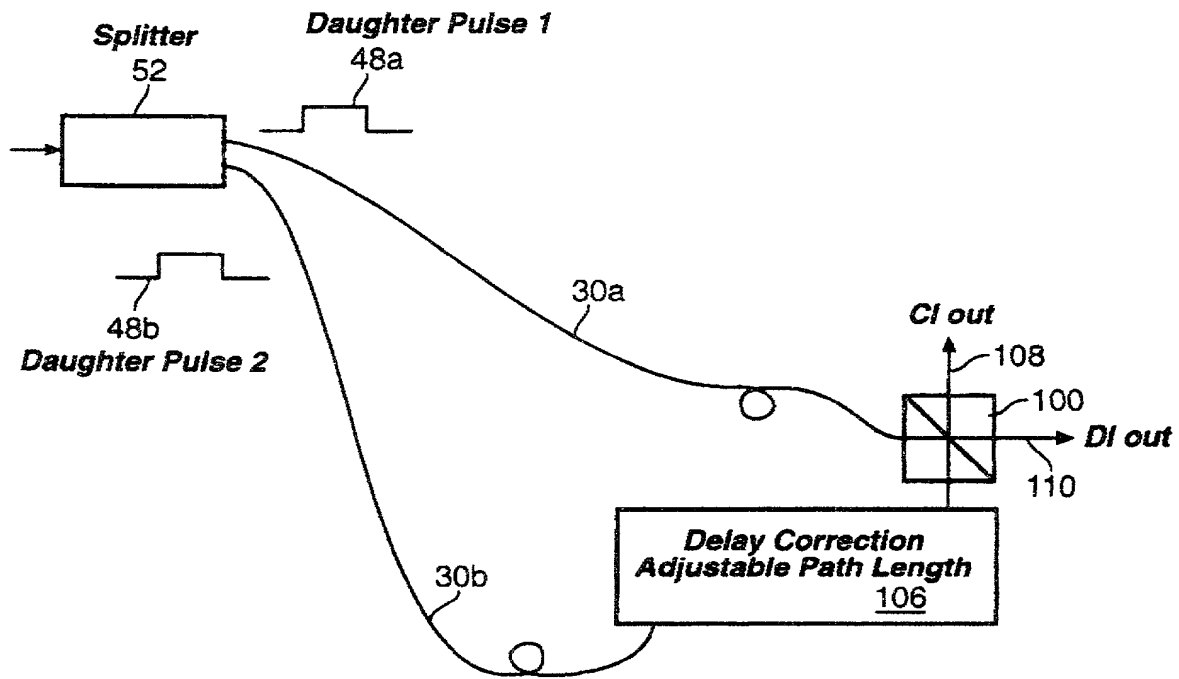
Fig. 24



Compound Multiplexing with DDM External

Fig. 25





Multiple Delay Path

**Integrated Delay and
Delay Correction**

FIG. 27

Photonic NRZ Interface

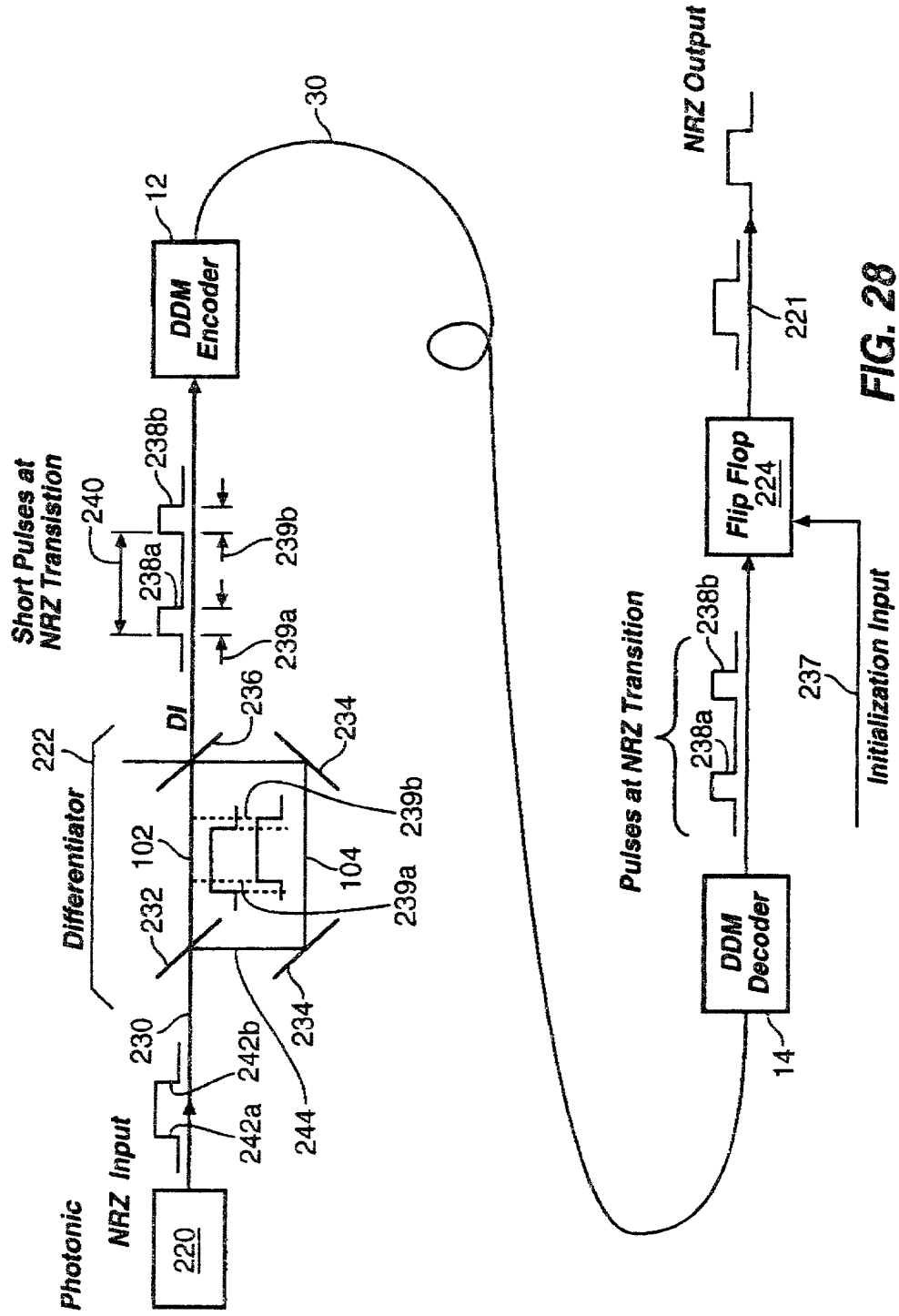


FIG. 28

28/50

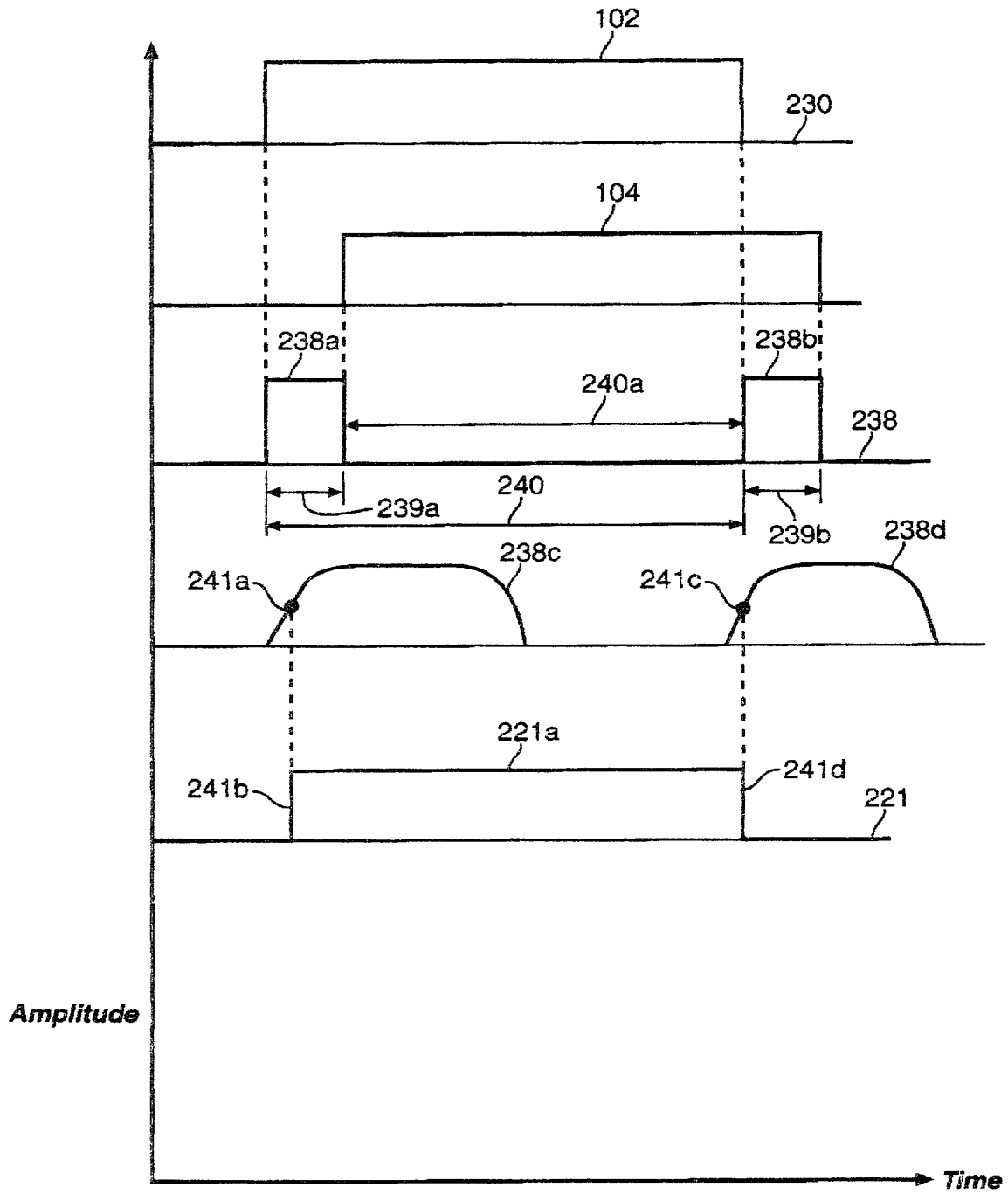
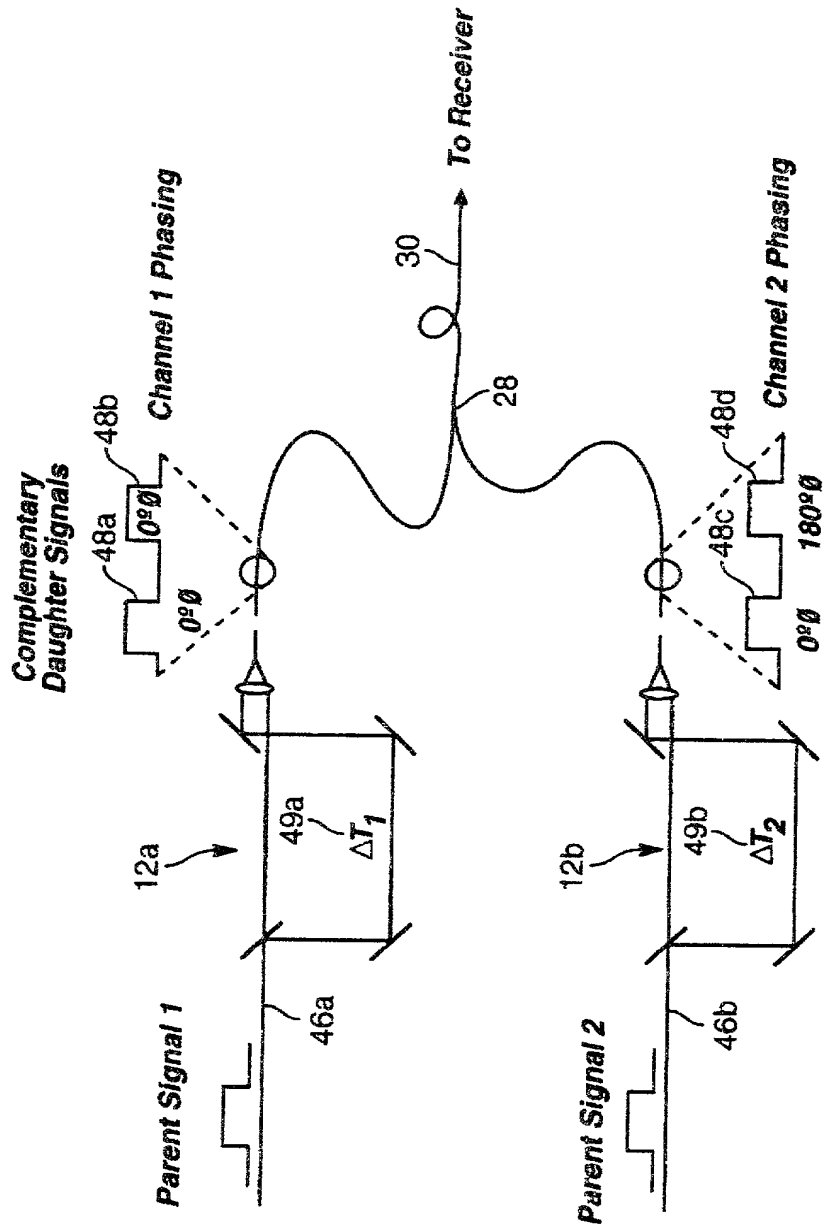


FIG. 29



Phase Sequenced Dual Channel Encoder

FIG. 30

Phase Sequence Timing

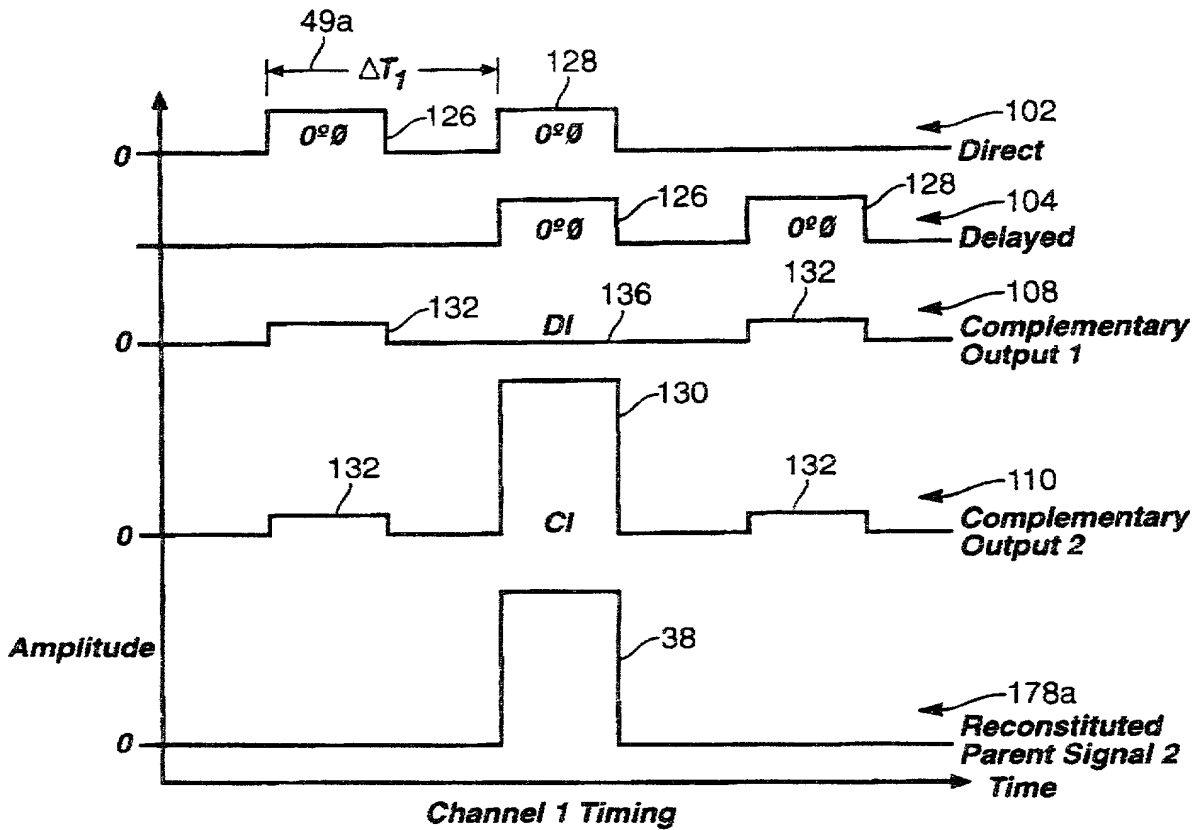


FIG. 32

Phase Sequence Timing

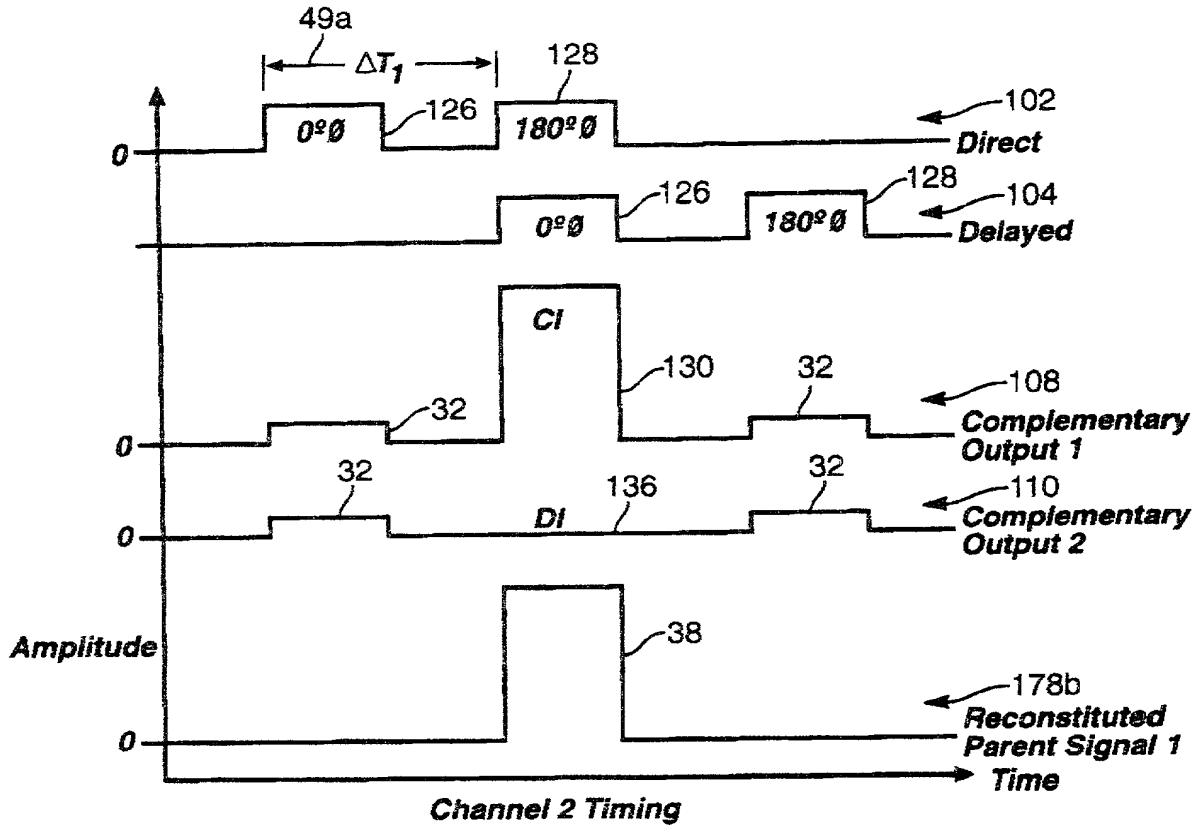


FIG. 33

	<i>Phase of Direct Signal</i>	<i>Phase of Delayed Signal</i>	<i>Quadrature Outputs</i>			
			<i>A</i>	<i>B</i>	<i>C</i>	<i>D</i>
46a → Channel 1	0	0	<i>CI</i>	<i>DI</i>	<i>C = D</i>	
46b → Channel 2	0	180	<i>DI</i>	<i>CI</i>	<i>C = D</i>	
46c → Channel 3	0	90	<i>A = B</i>		<i>CI</i>	<i>DI</i>
46d → Channel 4	0	270	<i>A = B</i>		<i>DI</i>	<i>CI</i>

245a 245b 245c 245d

FIG. 35

Quadrature Wave Forms For One Channel

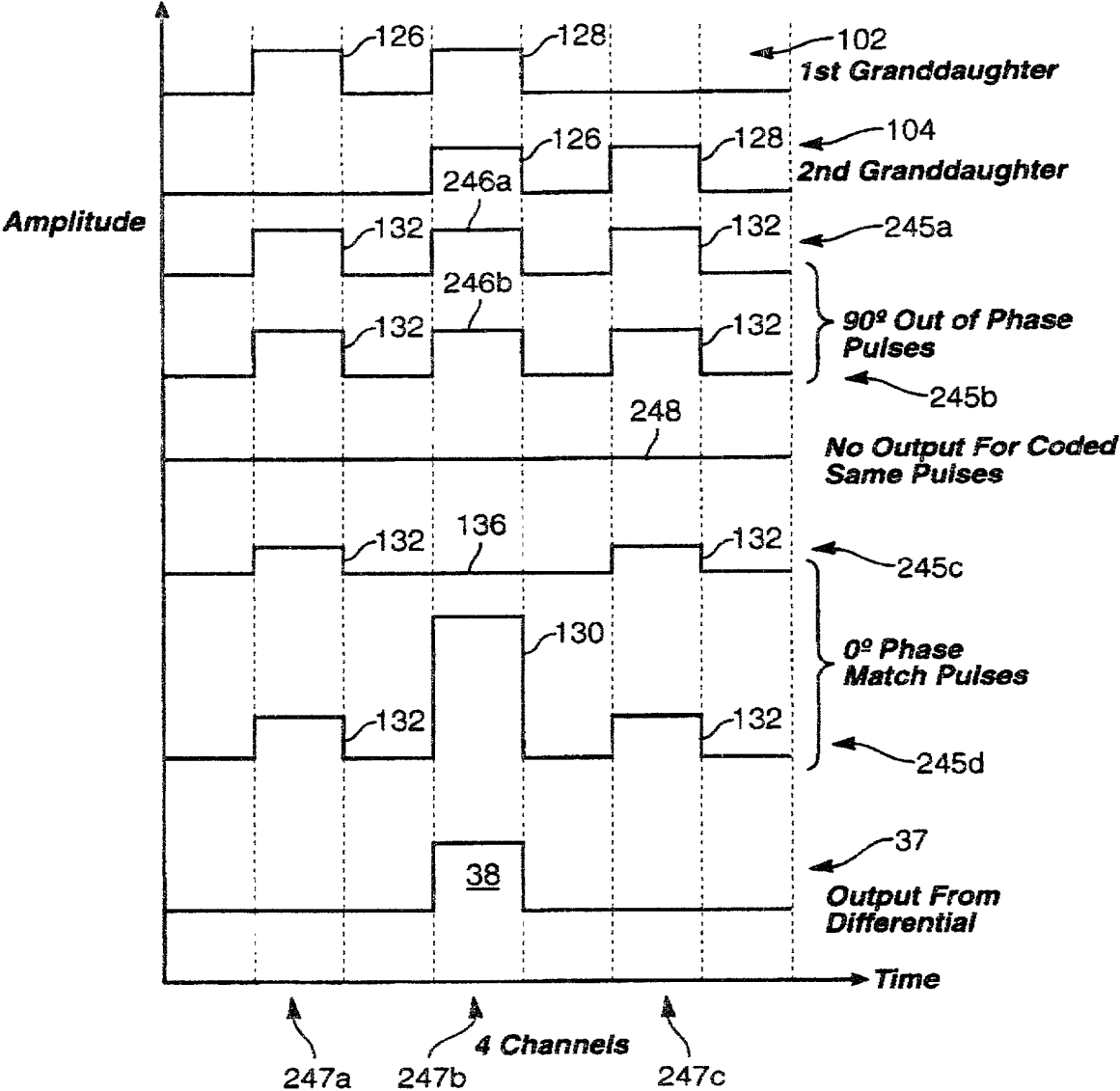


FIG. 36

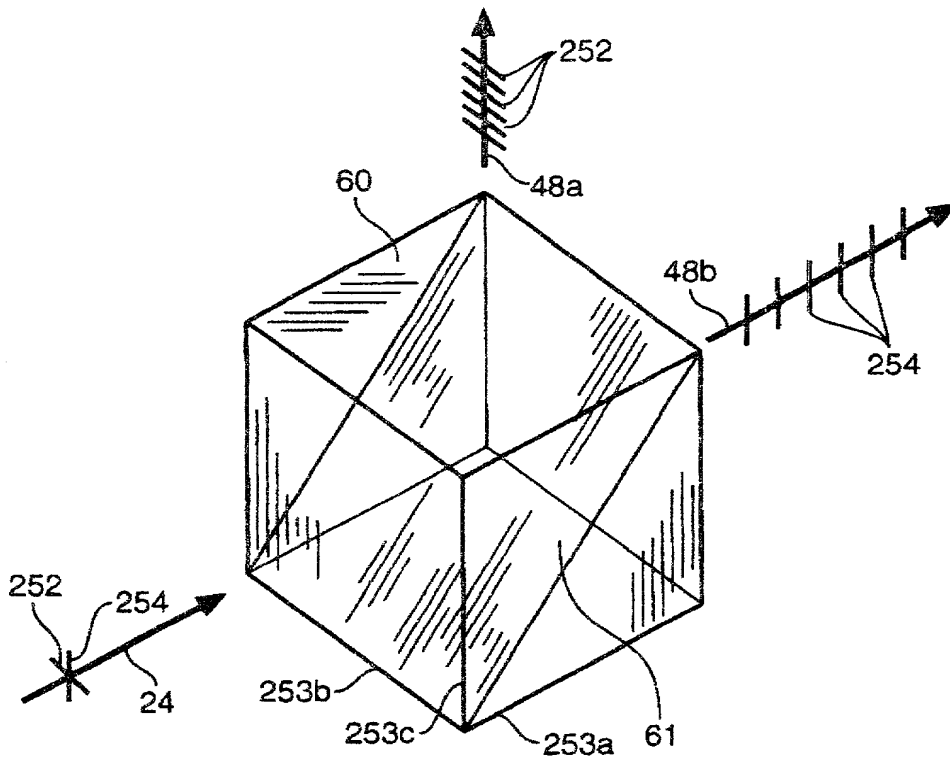


FIG. 37A

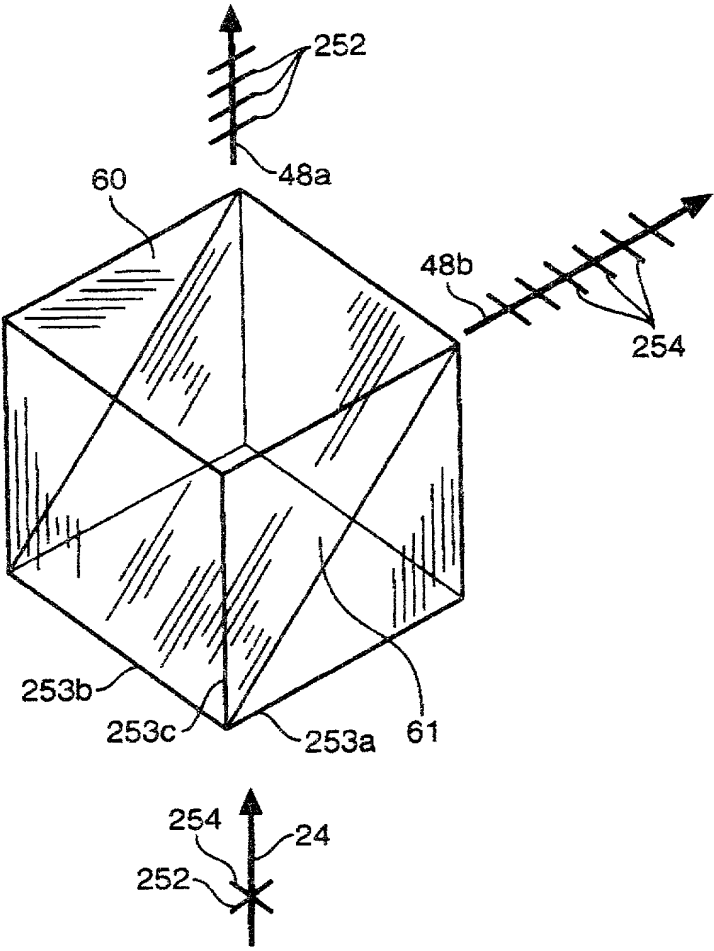
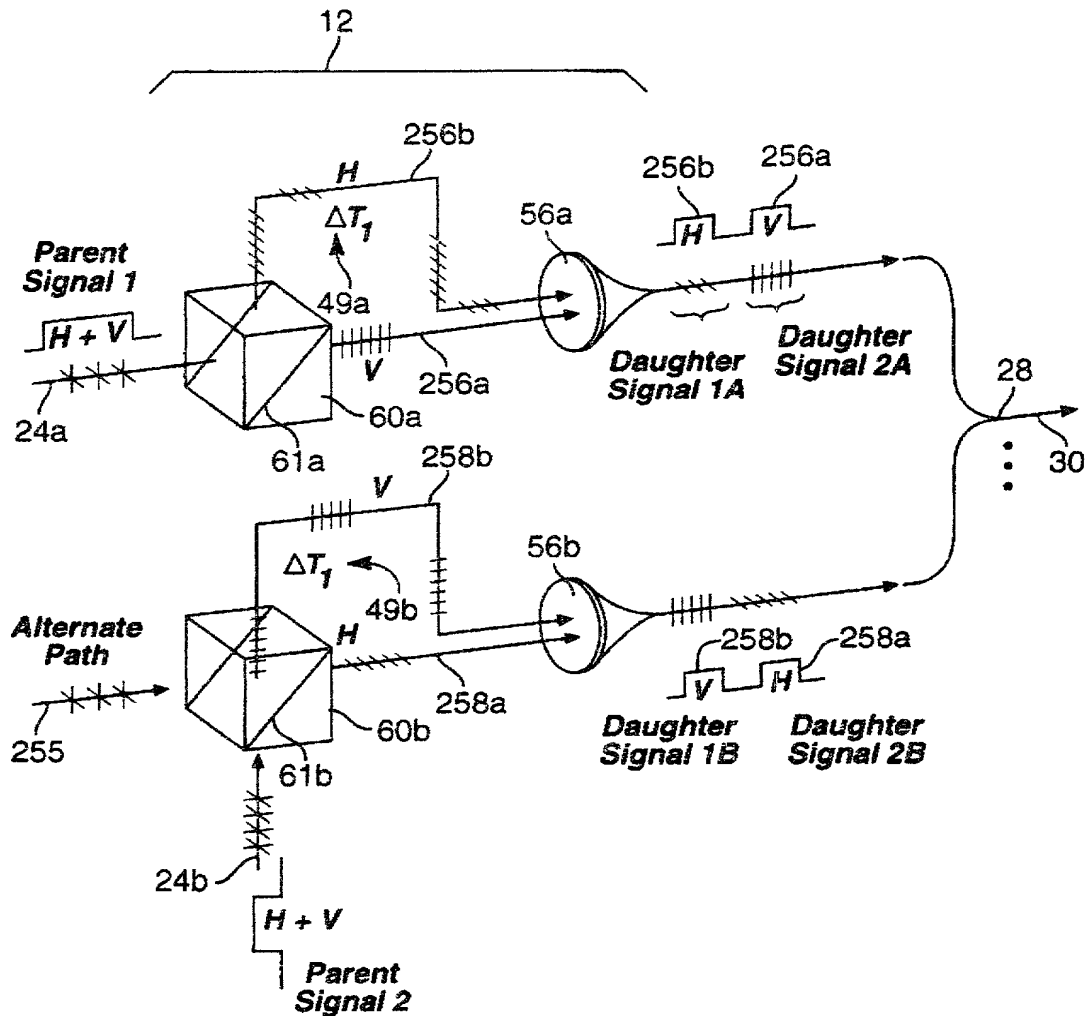
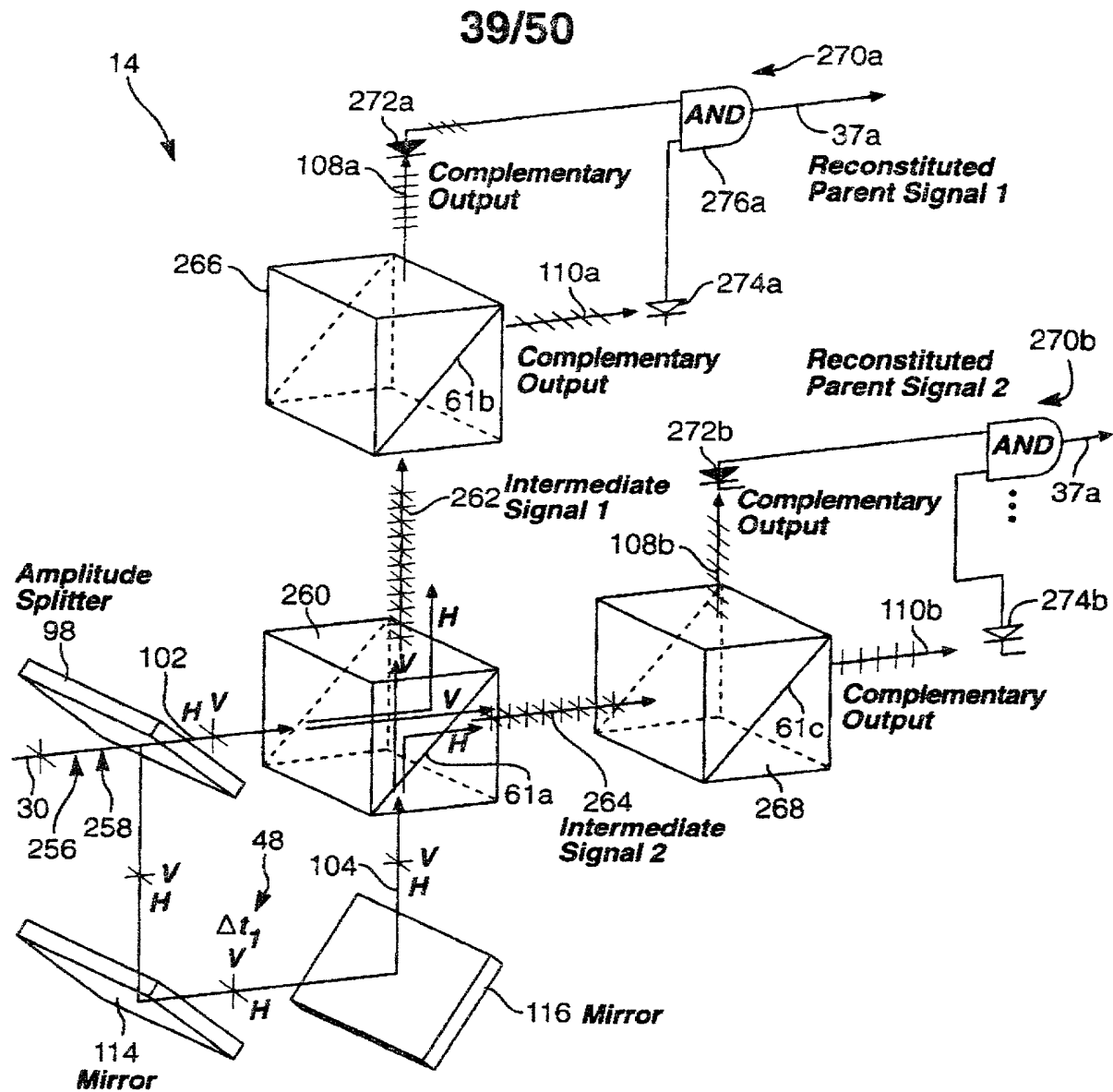


FIG. 37B



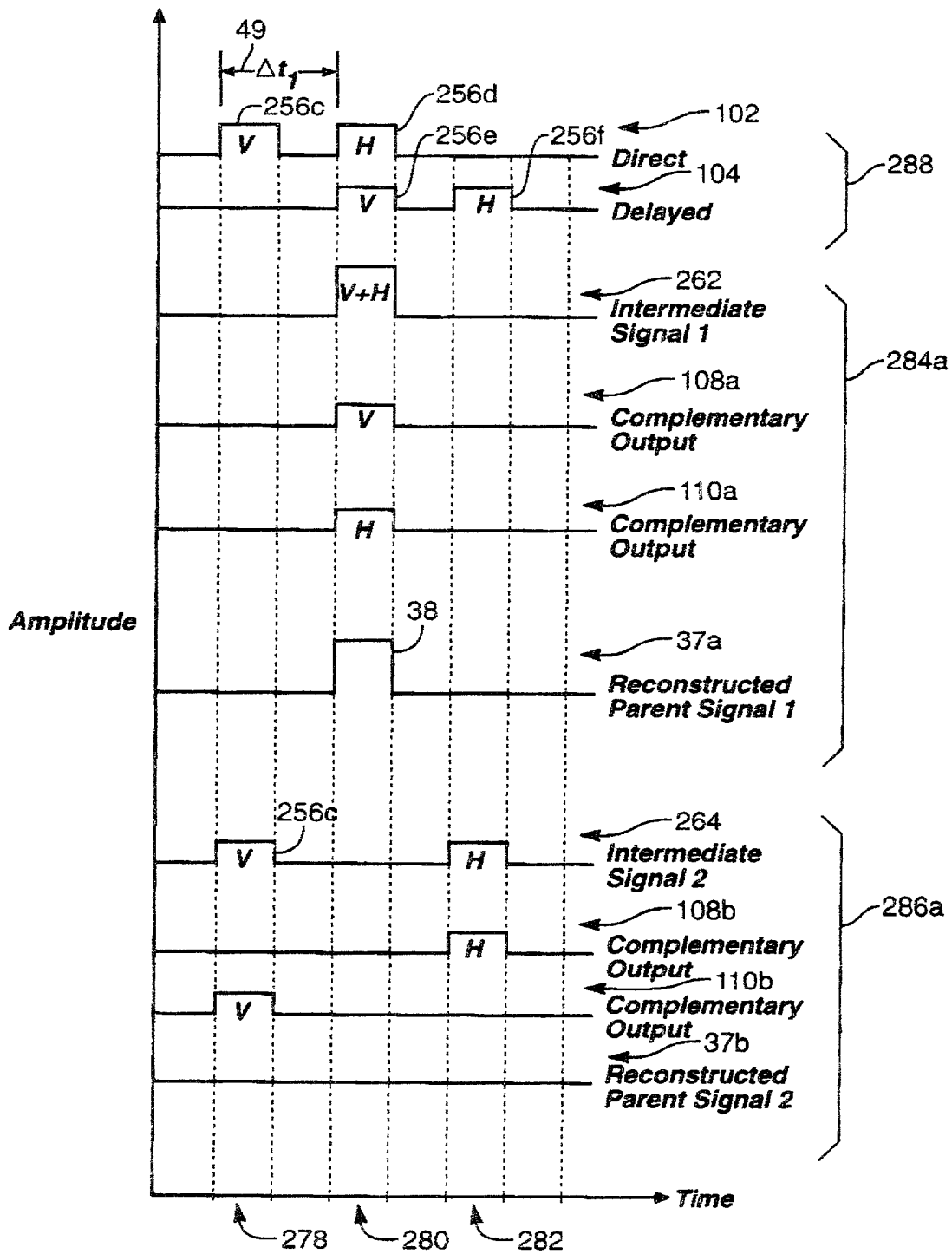
Double Encoder With Polarizations Sequenced to Differentiate 2 Channels Having the Same Time Delay Between Daughter Signals

FIG. 38



Double Decoder With Polarizations Sequenced to Differentiate 2 Channels Having the Same Time Delay Between Daughter Signals

FIG. 39



Polarization Sequenced Channel 1 Timing

FIG. 40

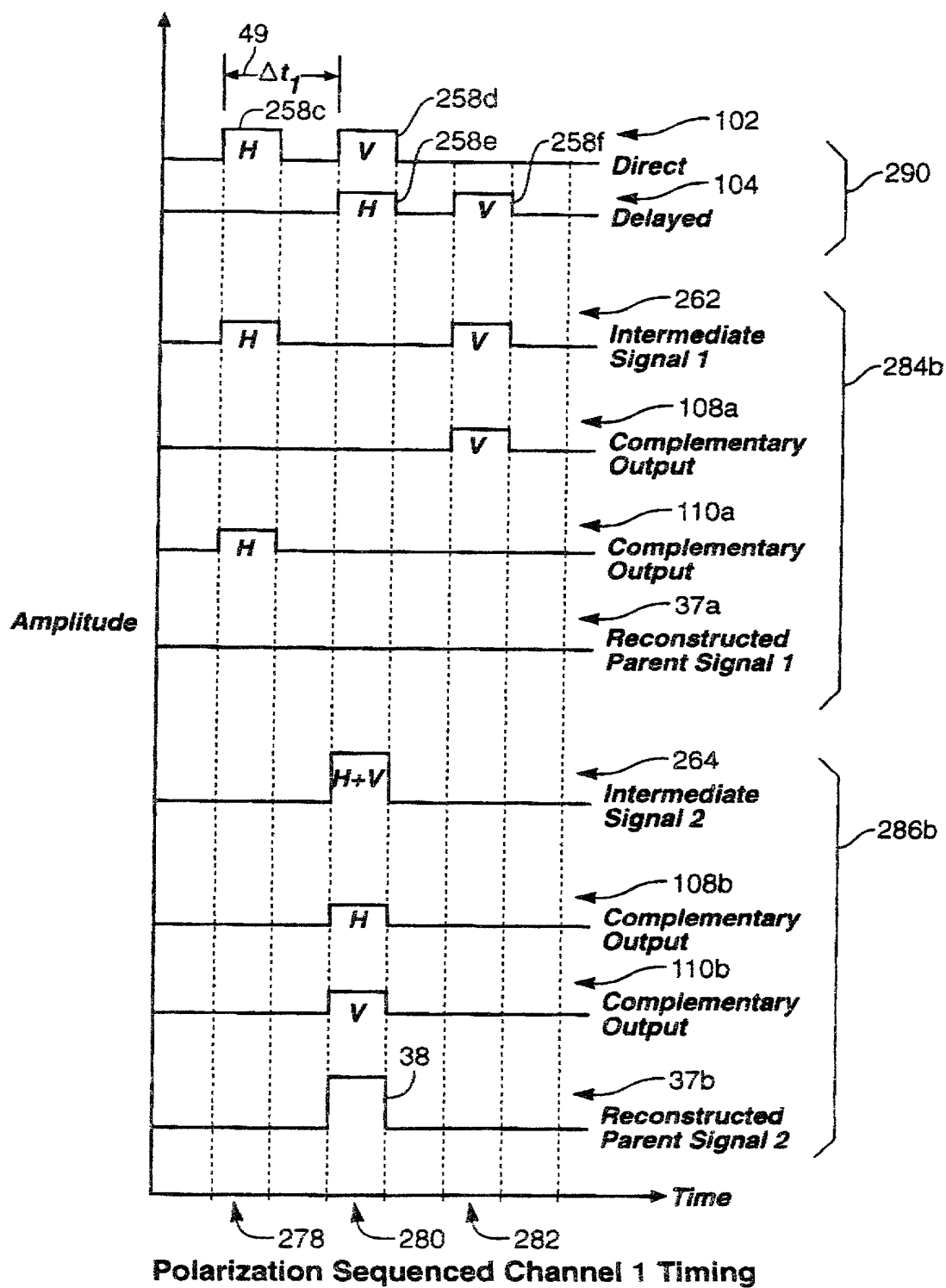


FIG. 41

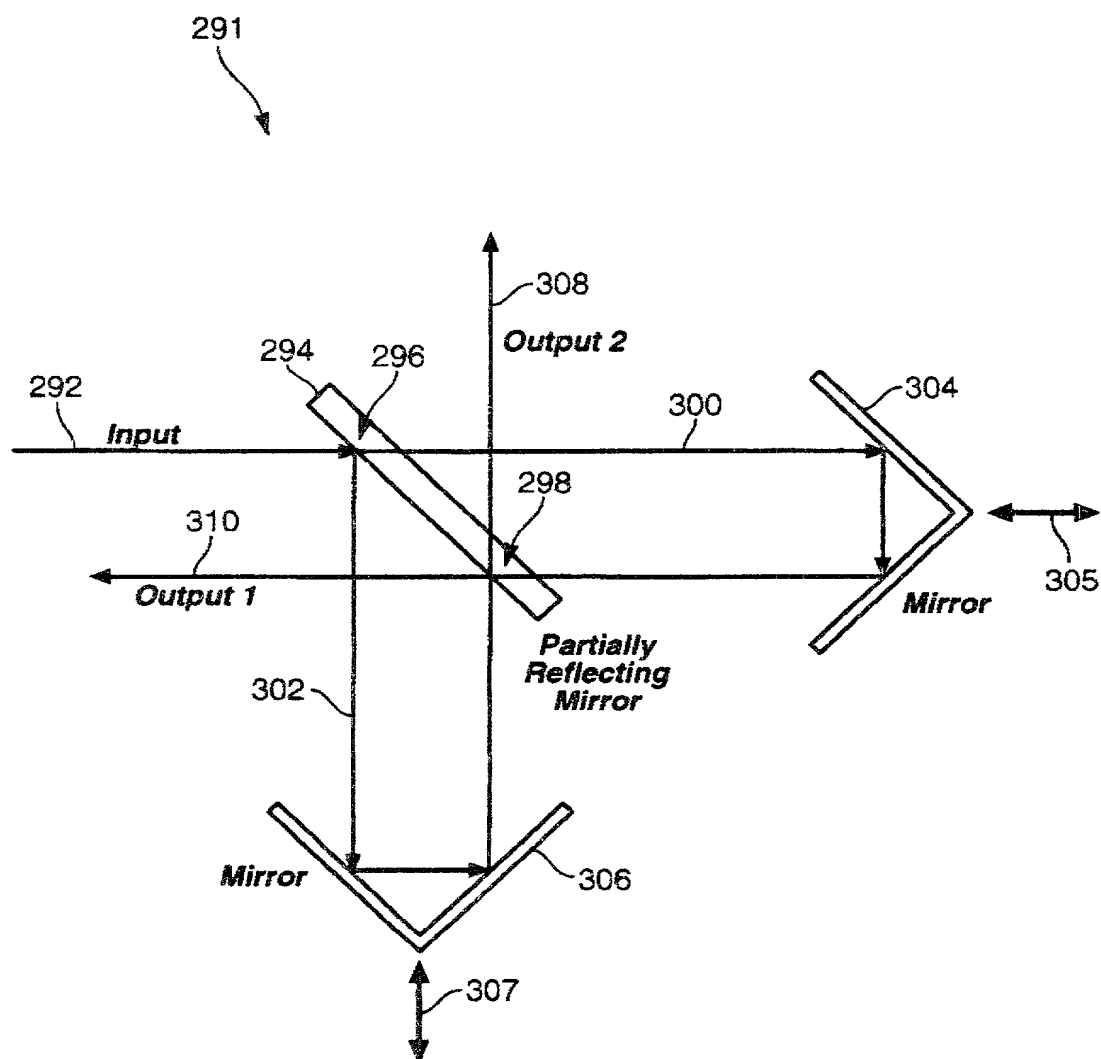


FIG. 42

43/50

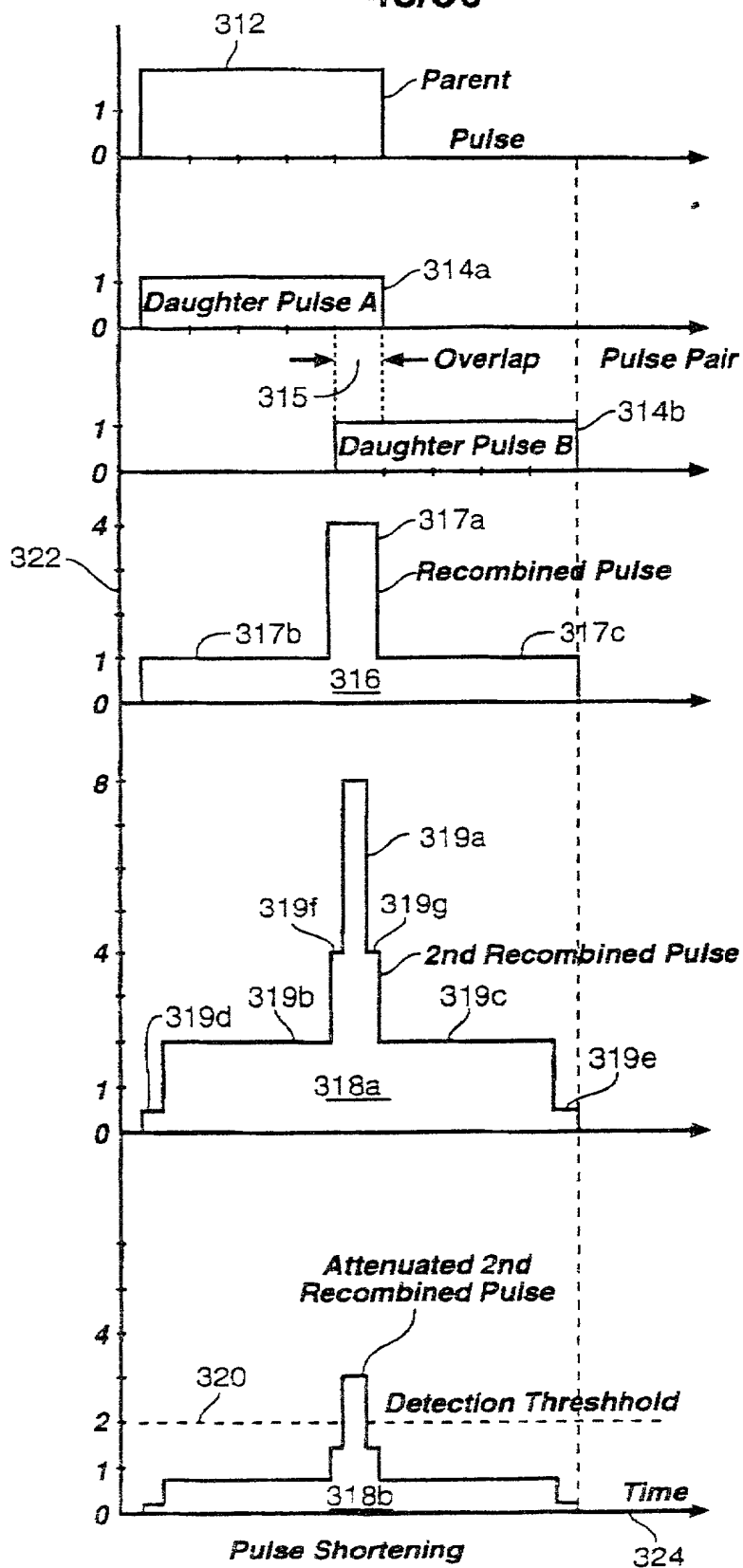


FIG. 43

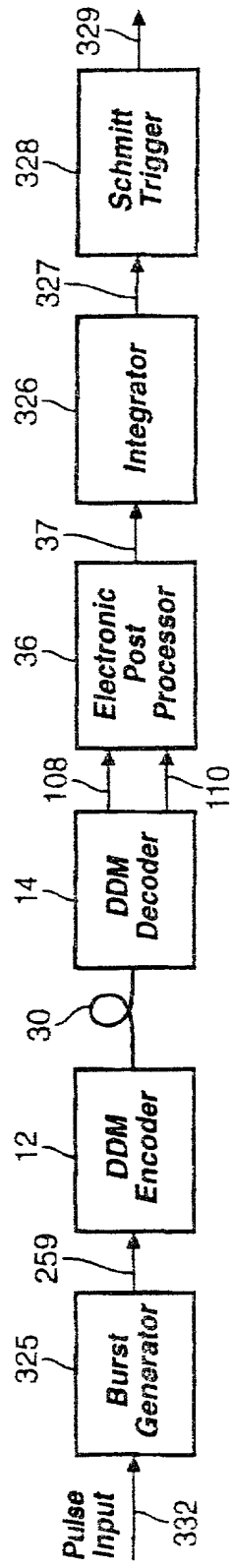


FIG. 44

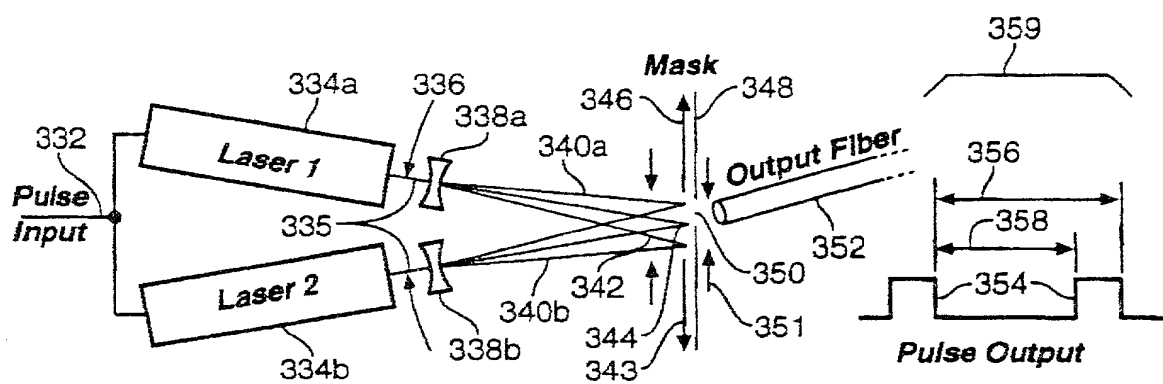


FIG. 45

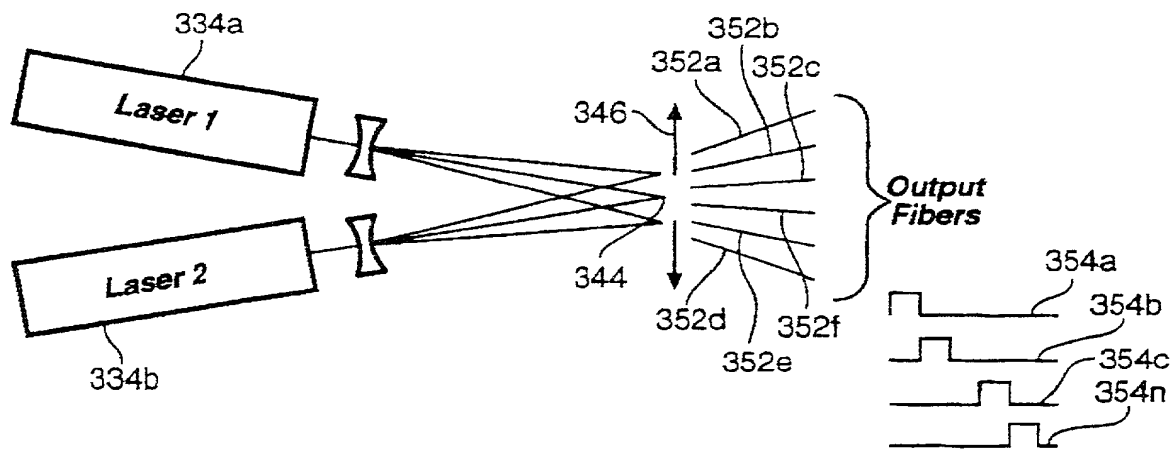


FIG. 46

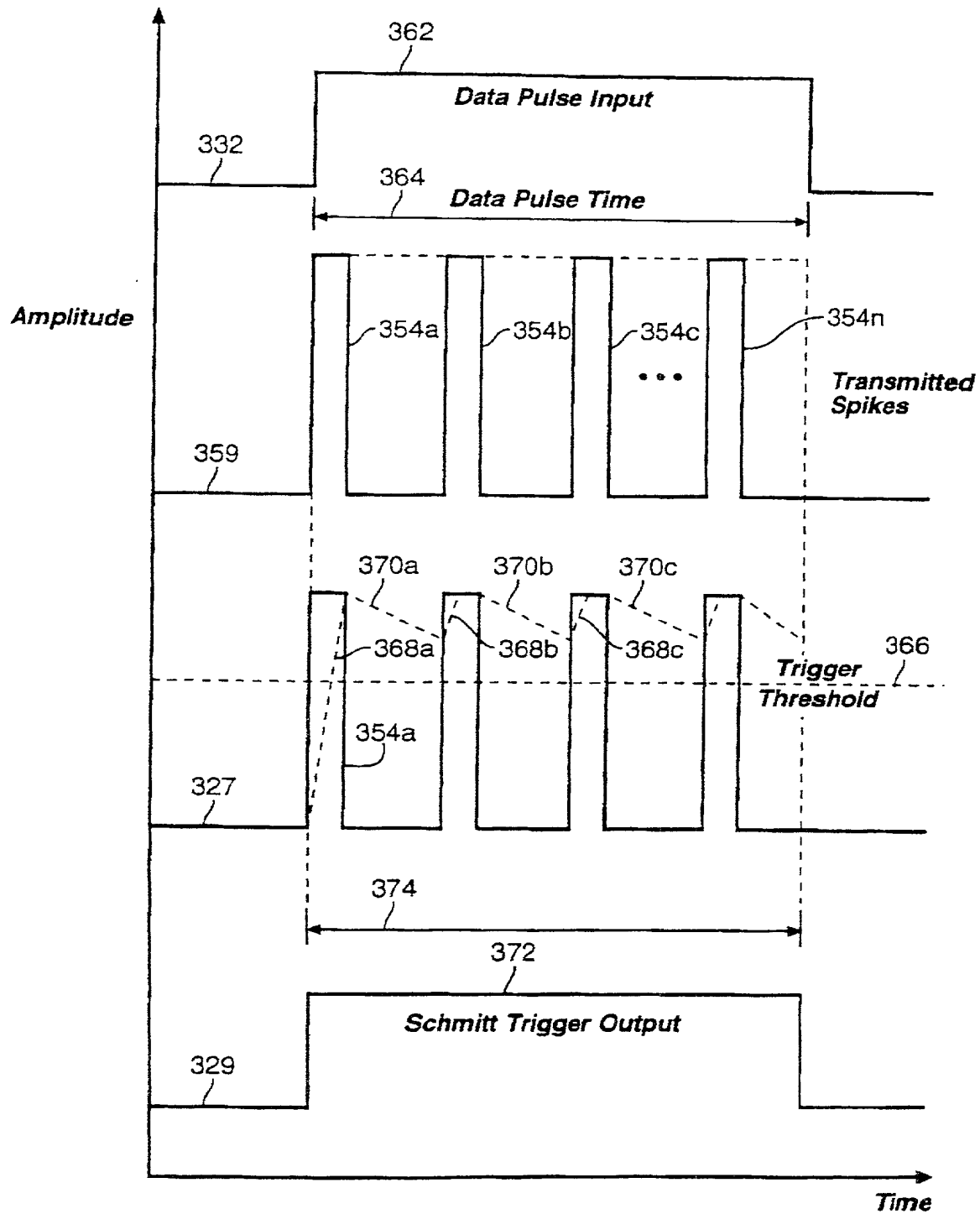


FIG. 47

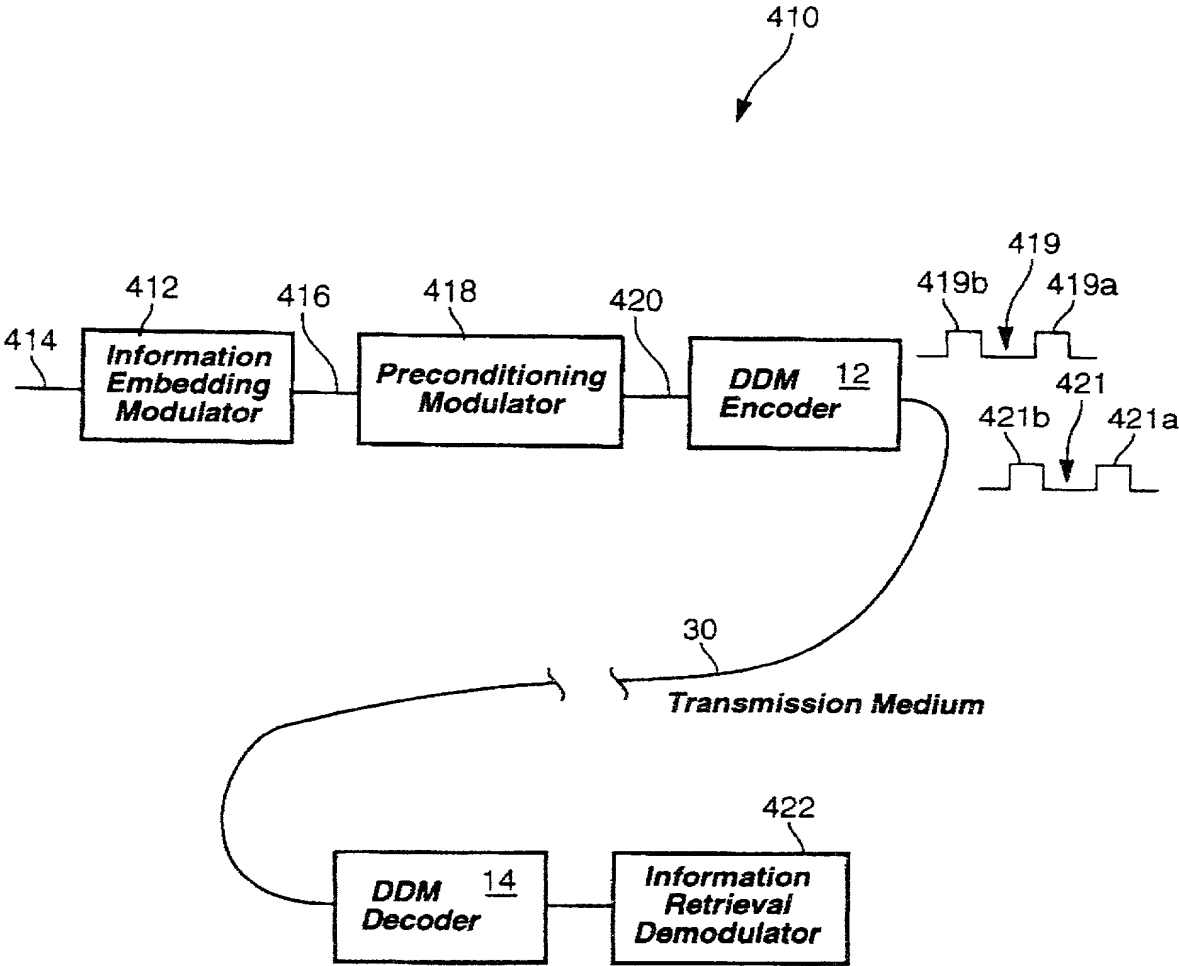


FIG. 48

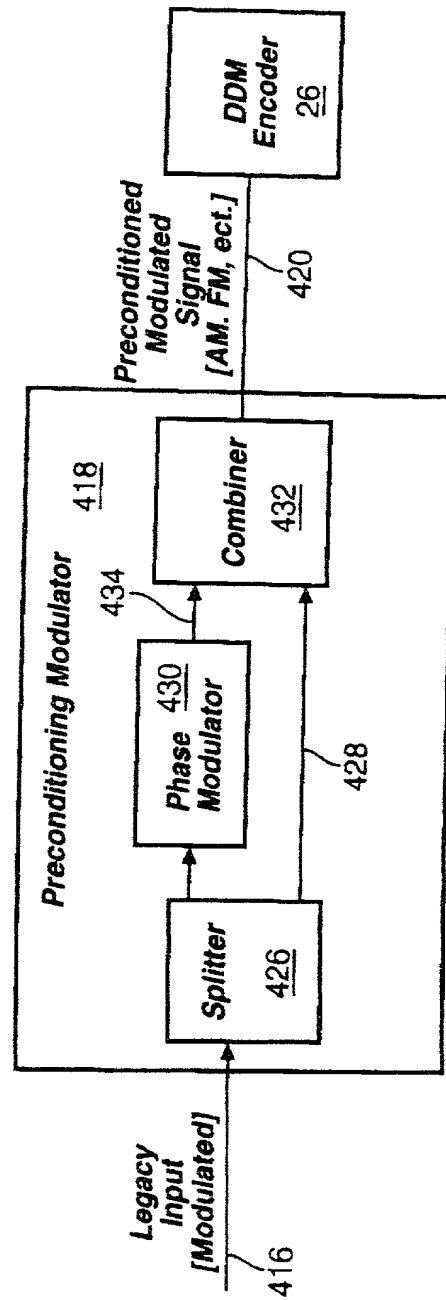


FIG. 49

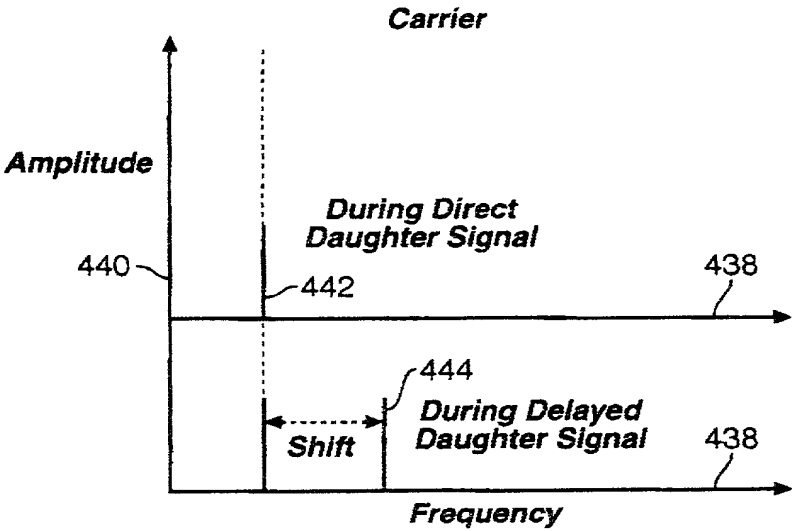


FIG. 50